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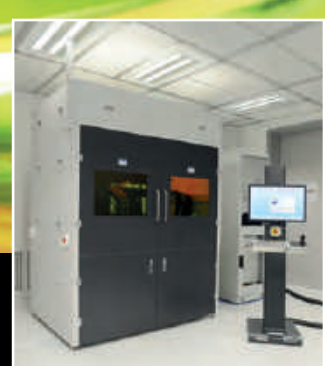

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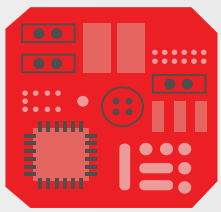

So, What's with the Bunny?

You may have noticed I've been carrying around a stuffed white bunny at trades shows recently. She was the star of the 2019 SEMICON West and SEMICON Europa slide shows. She even made the cover of this premiere issue of the 3D InCites Yearbook. If you're wondering what significance the bunny has, here's the story:

Bunny, as she is known, is the official SemiSister mascot. SemiSisters is a social organization I started several years ago for women who work in the semiconductor industry. Bunny belongs to one of the SemiSisters, who bought her in response to a request for a "booth bunny" to help out at industry events. "They didn't say what kind of bunny they wanted, so this is what they got," she explained. Bunny has become part of a campaign to highlight women who play vital roles across this industry.

Women in STEM

While women pursuing careers in science, technology, engineering, and math (STEM) are still very much in the minority, efforts to increase these numbers are growing. Women's organizations like the Society of Women Engineers (SWE), IEEE Women in Engineering (WIE), SEMI's Women in Semiconductors (WIS) initiative, the GSA's new Women in Leadership (WIL) program, and others, all exist to support these women, and to recruit more to STEM fields. Moreover, many companies have realized the benefits of an inclusive and diverse culture and are finding ways to foster this in their workplace.

In November 2019, I was invited to speak on the topic, *Corporate Cultures that Promote Women in Tech at the Society of Women Engineers* at the Society of Women Engineers in Sazburg, Austria. During my talk, I highlighted the efforts of Cornell University College of Engineering, last year's SemiSister Award recipient, for achieving parity in its class of 2022. (You can read more about this in Paul Werbaneth's article *Diversity, Parity, Prosperity: Perspective of an Industry Veteran* on page 41), I also shared best practices of Brewer Science; FRT, a Formfactor Company; and SPTS Technologies, a KLA Company, who were nominated for the SemiSister Award because of their efforts.

For example, at Brewer Science, 40% of its executive team are women. Overall, the company Averages 10-25% more women in technical jobs, leadership roles, and total workforce than most technology leaders in the semiconductor industry. The company does a considerable amount of community outreach to promote STEM education, such as offering a summer internship program for teachers who then utilize the skills they learn in classrooms.

At FRT, employee representation comes from 17 different countries of origin, 33 percent of which are women between 23 and 60 years. The company's hiring strategy is completely independent of gender or sexual orientation. Unique characters are underlined with positive appreciation, and individuality is encouraged. (Learn more about FRT's culture in this issue's cover story: 25 Years Perfecting the Art of Metrology, page 18.)

Finally, at SPTS, 22% of recent graduates hired and 15% of the apprentices are women. The company is focusing on increasing the number of female recruits through more female representation in recruitment material and events. The company is also involved in a Women in STEM initiative with the Welsh Government and participate in a STEM Ambassador program. Enhanced benefits to increase retention, including maternity and paternity leave and flexible work hours for all, has resulted in 100% of employees returning after maternity leave.

I'm proud to say that all of these companies are official members of the 3D InCites Community.

Women Not in STEM

But what about the scores of women who work in other roles in the semiconductor industry that don't require a STEM degree? This can be a tough crowd to break into when you don't know the lingo. I should know. I'm one of them. That's where SemiSisters comes in. We don't care if you're a female CEO, or her executive assistant. And we don't care if you have a Ph.D. in chemical engineering or a bachelor's degree in communications. We are all passionate about what we do and the roles we play, and we are here for you all. And that's why Bunny is on the cover of The Yearbook. I hope you enjoy the issue!

SEMI Standards in 2019

By James Amano, SEMI

The first SEMI Standards Committee was formed in 1973 to address silicon wafer dimensional specifications. At the time, there was a proliferation of over 2000 different wafer specifications, leading to major inefficiencies for a fledgling industry. Wafer suppliers banded together under SEMI to solve this problem and rapidly developed consensus specifications for 2-inch and 3-inch wafers. By the mid-1970s over 80% of wafers being shipped conformed to these new standards.

Since that time, the SEMI Standards Program has saved the industry untold billions of dollars by defining interoperability specifications, guidelines, and test methods that have streamlined semiconductor manufacturing and ensured the smooth operation of hundreds of pieces of equipment.

The 1000th SEMI Standard

The Program recently reached a major milestone, with the development of our 1000th Standard, *SEMI S30: EHS Guideline for Use of Energetic Materials in Semiconductor R&D and Manufacturing Processes*. Given the major contributions that SEMI Safety Guidelines have made to the industry, it's only fitting that our 1000th Standard comes from our Environmental Health and Safety (EHS) Committee.

Many semiconductor manufacturing processes require extremely reactive chemistry. Some process chemicals used are hazardously exothermic, pyrophoric or water reactive. While control procedures are in place to minimize the risks of such materials, new and emerging materials, some with unknown properties, have been introduced into manufacturing, causing potential risks for fire or explosion, which could release toxic chemicals into the environment.

From the period of 2011 – 2014, over 70 incidents were reported related to the use of new energetic compounds, causing loss of life, significant facility damage, and production business interruption. This spurred leading semiconductor device manufacturers, including GLOBALFOUNDRIES, IBM, Intel, Samsung, SK Hynix, TI, and TSMC, to form the Energetic Materials EHS Task Force. This group was charged with establishing a comprehensive, international best-known methods safety guideline for safe use, handling, processing, and disposal of reactive hazardous materials that have or may exhibit energetic properties. Thanks to the active participation of device manufacturers, chemical suppliers, equipment manufacturers, and third-party evaluators, the industry now has SEMI S30.

Smart Manufacturing

SEMI Smart Manufacturing activities have played a key role in the development of the current industry, enabling highly adaptive, self-diagnosing, and interoperable fabs. SEMI's suite of Equipment Data Acquisition (EDA) Standards define high-speed data publication from any manufacturing equipment to any data consumer through web services with the goal of increased productivity, improved product quality, and reduced costs. Also known as "Interface A," these standards address many different aspects of data collection — equipment modeling, data transmission, encoding, collection, management, and more.

To support the industry's demands to collect more data from equipment at faster rates, the global Information and Control Committee is updating the EDA Standards to use newer and better technologies and practices. EDA Freeze 3 will identify a specific set of SEMI Standards and versions so that equipment suppliers, software providers, and fabs can share a common data collection infrastructure, which will provide a nearly real-time stream of data that can be used to optimize manufacturing.

2019 also saw new equipment communication standards tailored specifically for the high-brightness light emitting diode (HB-LED), printed circuit board (PCB) and surface mount technology (SMT) industries.

SEMI A3, Specification for Printed Circuit Board Equipment Communication Interfaces, was created to support smart manufacturing for PCB makers by providing ready access to the equipment interface across the PCB manufacturing process. The specification lays the foundation for a reliable and extensible information technology (IT) integration framework for PCB manufacturing based on proven standards using a multi-layered approach. The specification references existing SEMI standards as much as possible to realize these layers. However, a small set of restrictions has been defined to simplify their application in the PCB industry, thus improving the level of acceptance.

Although automation in LED fabs is starting later than automation in the semiconductor wafer fabs, it is rapidly progressing. Many LED fabs already use SEMI communication protocols borrowed from wafer fabs, but handling and movement of carriers and wafers in LED fabs are different for LED. *SEMI HB13, New Standard: Specification of Susceptors for HB-LED MOCVD Equipment Communication Interface*, defines data collection for tracking wafer activity when using a susceptor or a wafer carrier, building on the previously published *SEMI HB4 - Specification of Communication Interfaces for High Brightness LED Manufacturing Equipment*.

SEMI SMT Equipment Link (SMTELS) Standards provide various benefits, allowing for a higher level of connectivity and control capabilities for SMT assembly lines.

The newly developed SEMI A2, Specification for Surface Mount Assembler Smart Hookup (SMASH), builds on the general purpose advanced machine to machine (M2M)

interface *SEMI A1, Specification for Horizontal Communication Between Equipment for Factory Automation System*, providing an interface specification that replaces the conventional electrical interface with a network connection and adds data communication capability.

Back-End Progress

Activities at SEMI have traditionally focused on the front-end, but companies involved in the back end are increasingly realizing the benefits of developing global consensus, industry-wide SEMI Standards.

Panel level processing (PLP) incorporates a mix of liquid crystal display (LCD), PCB, wafer-level, and high-density interconnect tool sets, leading to a chaotic industry landscape. PLP has been projected to become a critical packaging process and manufacturers are increasingly driving their suppliers to provide panel-processing tools and materials to allow them to bring wafer-level precision to packaged processed on panel substrates. One of the barriers to its adoption is the lack of a standardized panel size (Figure 1).

SEMI 3D20 - Specification for Panel Characteristics for Panel Level Packaging (PLP) Applications, focused on external panel dimensions, which will accelerate the adoption of PLP by eliminating the need to customize equipment and processes for a variety of panel sizes. A follow-on effort seeks to standardize critical dimensions for the corresponding equipment interfaces, specifically the FOUP load port.

To further strengthen Smart Manufacturing capabilities supporting high-end packaging operations, revision work is underway on

Figure 1: At Fraunhofer IZM, the PLP consortium is working to determine the ideal panel size for standardization. (Image courtesy of Fraunhofer IZM)

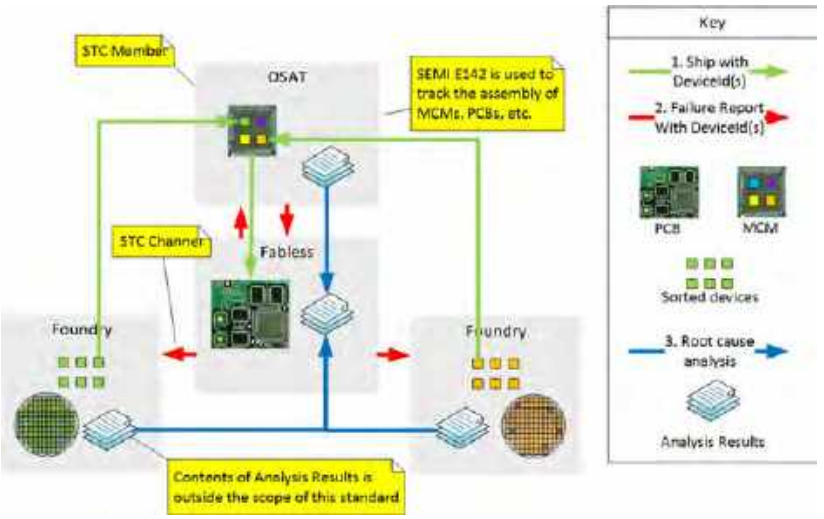

Figure 2: Diagram of standardized approach for traceable device-level identification throughout the IC manufacturing, test, and assembly processes to the point of use in the final system.

widely adopted standard, *SEMI E142: Specification for Substrate Mapping*, to enable tighter quality control requirements for advanced packaging and assembly. SEMI E142 defines the data items that are required to report, store, and transmit map data for substrates such as wafers, frames, strips, and trays. After this latest revision, SEMI E142 will define additional substrate types (e.g., PCB and panels) and how the physical substrates can be aligned with the E142 map data.

Traceability

The complexity and rigorous quality requirements of advanced technologies demands effective and efficient traceability across the microelectronics manufacturing supply chain. Sharing pertinent information enables faster and more detailed root cause analysis, critical for process improvement and excursion containment. Recent SEMI Standards work is helping establish a universal foundation to increase transparency and reduce traceability cost and complexity, enabling smart collaboration across the microelectronics supply chain (Figure 2).

The newly published *SEMI T23, Specification for Single Device Traceability for the Supply Chain*, provides a standardized approach for traceable device-level identification throughout the IC manufacturing, test, and assembly processes to the point of use in the final system. Suppliers and board-level manufacturers can use this unique identifier to communicate about a specific device for the purposes of performance assessment or failure analysis. The unique identifier will also allow manufacturing data to be sent backward and forward through the supply chain for data analysis.

Building on SEMI T23's capabilities, the Traceability Committee is now developing a new standard, *Specification for Counterfeit Prevention for the Electronics Manufacturing Supply Chain*, to provide secure and confidential authentication of parts as they flow between multiple segments of the supply chain.

2020 and Beyond

SEMI Standards have enabled the production of more than 2.2 billion wafers and 1.8 trillion IC devices. Referenced more than 10 million times in production fab purchases, more than 25 SEMI Standards, on average, are cited in each purchase order for semiconductor equipment and materials in the electronic manufacturing ecosystem.

In 2020, topics like big data, energy conservation, fab equipment information security, and power semiconductors will be the main focus of our task forces and committees, and additional topics are certain to emerge. As SEMI celebrates its 50th anniversary in 2020, the Standards Program will play a critical role as the industry becomes more complex and interconnected.

Dis-Integration is Underway

By Dr. Phil Garrou, Microelectronic Consultants of NC

We have known for some time that with scaling coming to an end, the industry would need to find another way to continue moving forward. One of the options is to actually "disintegrate" systems-on-chip (SoCs) into their functional parts and then connect these "chiplets" back together. Chiplets are not simply small chips. They cannot be used by themselves but are specifically intended to be interconnected together to build complete functionality. Thus, it is better to think of chiplets as a silicon intellectual property (IP) subsystem, designed to integrate with other chiplets through advanced package interconnect (usually micro bumps) and standardized interfaces. Building chips from pre-verified chiplets gaining traction as a way of cutting costs and reducing time to market for heterogeneous designs.

My first concepts of disintegration and chiplet technology came in the early 2000s when the industry began seriously looking at 3DIC technology and what advantages 3D would have over standard SoC technology. From the 5000-foot perspective, it was clear that what we were really heading towards was separation of functions, as shown in Figure 1 from a side I first used in 2005. At that time, I was espousing in my presentations and advanced packaging blog, IFTLE, that in the future, functions would be manufactured as separate chiplets, using the best technology and node, and recombined on high density substrates to form a multichip module with near SoC performance.

These thoughts were modified as it became clear that heterogeneous 3D stacking would be a complex undertaking (chiplet sizes, matching I/O, standard interfaces etc.) and would instead be proceeded by what is now called 2.5D integration, where the functions could be manufactured separately, at optimum technology and optimum node, and combined on a high density interposer.

The first commercial entity I saw express similar ideas was AMD's Bryan Black at Georgia Tech's Global Interposer Conference in 2011. Brian noted that the Southbridge at 22nm would probably be the last AMD chip impacted by scaling and that in the future "…separately

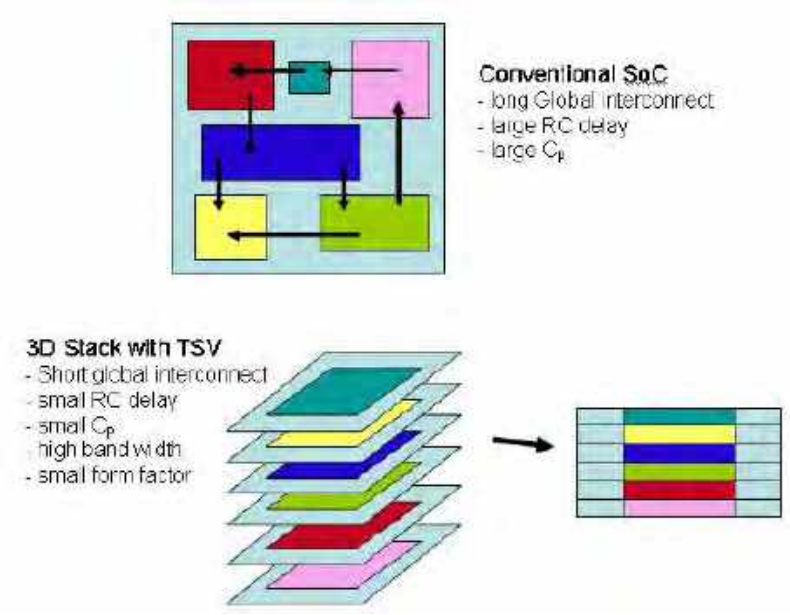

Figure 1: An early diagram of how SoC could be partitioned into separate functions and re-integrated vertically into a 3D stacked IC.

Figure 2: Diagram of SoC dis-integration by function.

fabricated functionalities would be combined vertically or horizontally on an interposer to form the final circuit function" (Figure 2).

Xilinx had already announced production of its 28nm Virtex 7 FPGA in 2010, but that's not what we are talking about now. Xilinx broke a large chip into four equal pieces and recombined it on an interposer to achieve higher yield and near equal performance. Here we are separating by function, optimizing process yield and recombining. The question was, would that ever be an economic solution, and could the current infrastructure ever support such a contrarian concept?

Marvell's MoChi

In 2015, Marvell announced their modular chip architecture ("MoChi"), which they described as a virtual SoC. Rather than integrating as many functions as possible into an IC (the SoC concept), the MoChi approach focused on splitting an SoC into chiplets of specific functions, that could be connected with each other without compromising the overall system performance. Although this was reportedly being commercialized in internal Marvell products, the technology did not gain traction or much attention outside Marvell.[1]

DARPA's CHIPS

In 2015, Dan Green and DARPA had similar yet slightly different thoughts from the DoD perspective.[2] The department of defense (DoD) was having trouble gaining access to the latest chip nodes and packaging technology. By definition, they would always have a high number of part types but low volume runs for each part. This was not exactly the type of orders Intel, TSMC, Samsung, ASE or Amkor were/are looking for. But, what if each piece of IP in a SoC could be

fabricated into small chiplets, tested and standardized so they could "talk" to other chiplets, and be available as standard chiplet parts at a given node?

Thus, the basic idea is that you have a library of chiplets. By assembling the required chiplets (functions) and connecting them using a standardized die-to-die interconnect scheme, you could develop new systems required by the DoD. In theory, the chiplet approach could be a fast and less expensive way to procure such devices. It's certainly been proven for SoC products that reuse of IPs have enabled people to create advanced designs in a much faster timeframe.

In theory, you could have a large catalog of chiplets from various IC vendors. Then, you can mix-and-match them to build a system. Chiplets could be made at different process nodes and re-used in different designs (Figure 3).

The DoD DARPA program, Com-

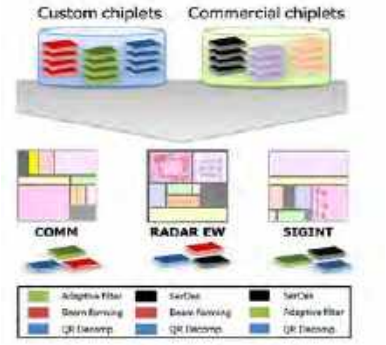

Figure 3: CHIPS enables rapid integration of functional blocks at the chiplet level.

mon Heterogeneous Integration and IP Reuse Strategies (CHIPS), began in 2017 involving various types of contractors/sub-contractors including Intel, Northrop, Micross , Ferric, Jariet, Micron, EDA suppliers Synopsys and Cadence, and several universities including Michigan, UCLA and Georgia Tech.

With chiplets, the designer could focus on designing at a higher level by integrating known and trusted chiplet functionalities, but there appeared to be two main obstacles that needed solutions before chiplet technology could be looked at as mainstream:

	Monolithic SoC	Chiplet on Substrate	Discrete IC on PCB
Design Cost	Highest design cost 7nm > $200 million	Less costly than monolithic SoC	Least expensive
Design Time	Longest design cycle 18+ months	Shorter design time 12 months faster to make derivative design	Shortest design time 6 months
Design Risk	Highest risk, including missing future features, having to do a redesign	Lower risk, can change out chiplets to add or subtract features, redesigns are simpler	Lowest risk
Performance	Highest performance, but some functions might not scale so would use larger design rule for that portion of the chip, leads to inefficient use of resources	Good performance, can use the most appropriate process for the function needed in the chiplet	Lowest system performance, problems with timing, latency, more complex PCB
Power	Possibly the lowest power consumption	Very close to the same power consumption of a monolithic SoC	Highest power consumption
Time to market	Longest	Quicker	Shortest
Product size	Smallest	Small	Largest

Figure 4: Pros and cons for SoCs, chiplets and traditional system design. (Source: Semico Research)

Chiplets from different sources MUST have standardized interfaces and communication protocols.

Currently at least three options are under serious evaluation. Intel has developed AIB and MDIO, TSMC has developed Lipincon, and the Open Domain-Specific Architecture (ODSA) has created the CDX (Chiplet Design Exchange) to standardize design.

Known-good Die (KGD)

Using chiplets takes us back to the KGD conundrum from the early MCM days in the 1990s. The purchaser of a chiplet, requires virtually 100% yield, i.e. a fully tested and qualified KGD. Also ensuring that the connections between the chiplets on the substrate/board are properly tested, is essential.

Several companies are working on a variety of interposers and bridge technology, which is less expensive than an interposer. Intel already has its embedded multi-die interconnect bridge (EMIB), and Samsung has announced a redistribution layer (RDL) bridge for wafer-level packaging.

Commercialization

Both technically and financially, the industry's traditional method of building increasingly larger chips has become less and less appealing. So, major semiconductor companies are designing products that break the larger designs into smaller pieces ("chiplets") and combine them. Comparison of monolithic vs. chiplet solutions are shown in Figure 4.

In the last 24 months or so we have seen AMD, Intel, TSMC and Samsung adopt chiplet solutions.

AMD

In 2017 AMD used chiplets in their "Zen 2" architecture to develop the Epyc server processor "Naples". AMD engineers estimated an SoC design would have more than doubled the manufacturing cost and significantly increased the development time. AMD is now deploying its "Zen 2" chiplet technology in Ryzen 3rd Generation consumer CPUs (Ryzen 3000s) and AMD's next generation enterprise EPYC processor, known as Rome.3

The IO die for the EPYC Rome processors uses Global Foundries' 14nm process, however the consumer processor IO dies (which are smaller and contain fewer features) are built on the Global Foundries 12nm process. The EPYC Rome processors, built on these Zen 2 chiplets, will have up to eight of

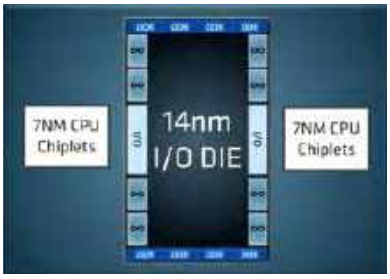

Figure 5: Schematic of EPYC Rome processors. (Source: AMD)

them, enabling a platform that can support up to 64 cores. As with the consumer processors, no chiplet can communicate directly with each other — each chiplet will only connect directly to the central IO die. That IO die houses links for eight memory channels, and up to 128 lanes of PCIe 4.0 connectivity (Figure 5).

The IO die controls off-chip communications, housing PCIe lanes for the processor, memory channels, and links to other chiplets or other CPUs.

The consumer processors, Ryzen 3rd Gen or Ryzen 3000, will be offered with up to two chiplets for sixteen cores.

AMD is using "Infinity Fabric" (IF), (their interconnect protocol, NOT something Thor and Iron Man acquired from Thanos) to connect chiplets and the DDR DRAM interfaces. The IF protocol can run on any hardware in which it is implemented. IF can run through PCB traces, an interposer or EMIB, as long as both connected dies support it.

Separating CPU chiplets from the I/O die has its advantages because it enables AMD to make the CPU chiplets smaller thus using less 7NM technology theoretically making the module less expensive to manufacture.

Intel

Intel's EMIB technology basically uses small silicon interposers to connect (i.e. bridge) two chiplets through microbump (~ 55um pitch) interconnect.[4]

The EMIB is embedded into a high-density PCB packaging substrate. Intel claims this results in lower cost since the whole substrate does not need to be high cost 2.5D silicon, but some outside Intel are not convinced that these specialty PCB substrates with embedded silicon are as simple to make or cheap to buy as Intel infers. Intel reports that they currently have two solutions based on EMIB.

Kaby Lake-G integrates an AMD Radeon graphics processor unit (GPU) with a high bandwidth memory (HBM) memory stack and an Intel computer processor unit (CPU) chip (Figure 6). Kaby Lake uses an HBM interface inside the package to integrate the GPU and HBM and PCI Express, a standard circuit-board-level interface, to integrate the GPU and the CPU.

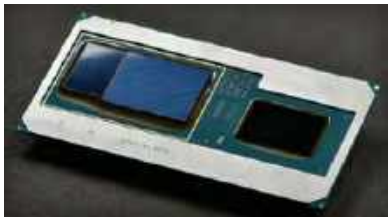

Figure 6: Kaby Lake is one of Intel's chiplet solution based on EMIB technology.

The Stratix 10 FPGA has an Intel FPGA and six chiplets (Four high-speed transceiver chiplets, and two HBM chiplets) and they are all assembled in a package (Figure 7). This example integrates six different technology nodes from three different foundries.

Figure 7: Stratix 10 is the second Intel chiplet solution based on EMIB technology.

Stratix 10 uses the Intel-developed Advanced Interface Bus (AIB), which was created for this product as the high-bandwidth, logic-to-logic interconnect inside the package. The AIB interface can be used both with Intel's EMIB interconnect solution and other solutions such as silicon interposers. AIB is currently the standard interconnect of choice in DARPA's CHIPS program.

Chiplet Standardization

To get widespread adoption of chiplet technology we must have I/O interface standardization. i.e. a chiplet made by company A must be able to talk to a chiplet made by company B. The DARPA CHIPS program has focused on the Intel AIB protocol. Recently, TSMC, who is fabricating chiplets for AMD announced its "Lipincon" protocol. [5]

In September 2019, the Chiplet Design Exchange (CDX) (zGlue, Ayar Labs, Avera Semi, ASE, Cadence, Netronome, and Sarcina) announced, as part of the Open Compute Project, a subproject to standardize design automation for the impending chiplet marketplace. The group is tasked with standardizing machine-readable chiplet models to enable chiplet catalogs and provide reference flows for the development of chiplet-based modules.

CDX plans to create a proof-of-concept based on PCIe while developing its PHY, protocol and other specifications. The group also aims to define a business flow for chiplets and define a test certification for known good chiplets. EE Times reports that the group "appears to have rejected Intel's AIB protocol as being too limited in data rates and pinouts." [6]

In conclusion, disintegration of traditional SoC technology appears to be underway!

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Chiplets: The New Era Begins

By E. Jan Vardaman, Tech-Search International, Inc.

The semiconductor industry has entered a new era and the role of design, including the package, has become increasingly important. No longer can the industry count on monolithic integration to achieve the economic gains of the previous era. New packaging solutions are being adopted to achieve the economic advantages that were previously met with silicon scaling. The role of heterogeneous integration, especially chiplets, is pivotal in this new era. In fact, TSMC indicates that the use of chiplets will be one of the most important developments for the next 10 to 20 years.

Drivers for the New Era

In the mid 1960s, Intel's Gordon Moore observed that by shrinking transistors, it would be possible to double the number of transistors that fit onto an integrated circuit every year (revised to roughly every two years) providing a cost advantage to scaling. With the high cost of monolithic integration, this observation no longer holds true to the same extent it once did. Smart packaging is the new way to extend this observation and the use of chiplets has become key.

What's a Chiplet?

A chiplet is a functional circuit block and includes reusable IP blocks. It can be created by partitioning a die into functions and is typically attached to a silicon interposer or organic substrate today, but new options are emerging. TSMC argues that the demand for chiplets is driven by the need for a more cost-effective solution, the reuse of IP, and new test flows. A cost reduction is possible because the die functions, such as I/O control, are split out. These die functions are more difficult to scale, requiring more time and money. Cost reduction is achieved by chip integration. With chips divided in two, the split chips can be stacked to provide a 20 percent cost improvement. Chip partitioning also improves time-to-market. The chiplet is not a new idea, but EDA tool improvements are making new architectures possible.

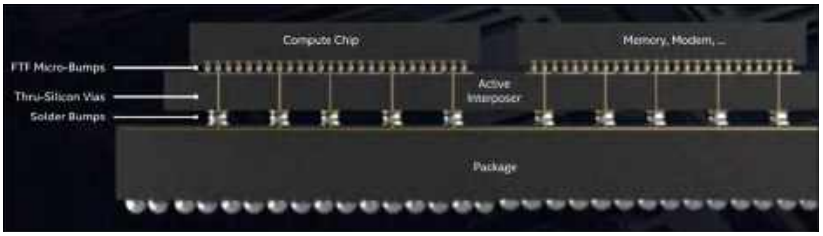

Figure 1. Foveros technology with 3D face-to-face stacking. (Source: Intel.)

TSMC

TSMC proposes its bumpless System on Integrated Chip (SoIC™) as one chiplet solution. The SoIC™ is a 3D structure formed by stacking logic, memory, or both chip types on an active interposer with TSVs. A chip-on wafer (CoW) process is used and the process can handle <10µm bond pad pitch between chips. The chips, with or without through silicon vias (TSVs), are bonded onto the wafer containing the active interposers using a hybrid bonding process. The 3D chip with TSV SoIC™ also uses through dielectric via and CoW bond. TSMC reports that the SoIC™ structure with its higher density bonding provides better signal integrity, power integrity, and lower communication latency with greater bandwidth than a conventional 3D IC using TSVs and 40µm pitch micro bumps. Lower insertion loss, important for 5G applications, is reported. Lower parasitics and low IR drop is reported. Finer interconnect pitch is possible and there is less concern with CPI because there are no bumps.[1]

AMD

AMD's current chiplet solution uses a laminate substrate. AMD has shipped multiple versions of its server processor using chiplets. Up to eight 8-core processors are tightly coupled together on an organic substrate. The chiplets can be binned and speed-sorted before assembly in the package. At the system level, the multi-die package architecturally acts as if it were a monolithic die.[2] AMD's new architecture allows the chiplets to communicate with each other as well as externally, including power and ground management. This new architecture and future approaches will allow performance improvements that cannot be met with monolithic integration, including power consumption.

Intel

Intel's latest chiplet solution is called Foveros. It is a 3D integration technology as a form of heterogeneous system integration. Heterogeneous integration is defined as the integration of separately manufactured components into a higher-level assembly or system-in-package (SiP) that, in aggregate, provides enhanced functionality and improved operating characteristics. The technology uses a 3D face-to-face stacking process. In the process, logic dies are bumped and mounted on an active interposer next to memory or die with communication functions such as a modem. The active interposer can contain active parts of the system, such as the platform controller hub (PCH) that manages I/O for the system. The active interposer is mounted on a package substrate with solder bumps (Figure 1). While the first demonstration of the technology used micro bumps, future versions are expected to use hybrid or direct interconnect bonding without a bump.

The Foveros technology will give designers greater flexibility to mix and match IP blocks with various memory and I/O elements into new form factors. Mounting memory on

Continued on page 55

Why AI needs 3D Heterogeneous Integration

By Dean Freeman, FMTA

Artificial intelligence (AI) has been hyped as one of the new key drivers of the semiconductor business. At the past two SEMICON West events, much of the focus was on AI and not necessarily the equipment required to make semiconductors. The digitization of business, and then using that data to come up with a unique business solution is one key AI driver. Using data or pictures to teach a system how to recognize either a pattern or a photo and then react to that information and make a decision — such as opening a locked door or differentiating between a lamp post or a human in an autonomous vehicle — is driving a new generation of semiconductor systems.

Simplistically, AI is broken down between the learning or teaching part of the process or the inference or recognition part of the process. The teaching part requires a significant amount of compute power from both the processor and the memory, and typically needs the cloud or a server to accomplish this task. The inference part can be performed on silicon chips as simple as a 32bit Microcontroller (MCU).

At ARM TECHCON 2019, both ST Microsystems, and NXP demonstrated AI inference using a 32bit MCU. NXP argued that with the right configuration of MCU and memory, the system could do a bit of learning that would not depend upon going back to the cloud to re-teach the system. However, with the emergence of 5G and the ability to perform the deep learning at the edge, there is the need for chips or a chip set that can perform the deep learning closer to where the data originates. This is one of the key drivers for heterogenous integration: It will enable a small enough formfactor with enough power that can be placed near the data acquisition point to perform the learning, teaching, and inference with low enough latency to provide a compelling business solution at a reasonable cost.

Energy Demands of AI deep Learning

The deep learning needed for much of the AI takes a great deal of energy. At IEDM 2019, IMEC showed that current technologies have performance of < 10 Tops/W. These are satisfactory for deep learning operations in a server farm, but not fast enough or power efficient for learning at the edge. New and different device technologies are needed to improve speed at lower energy consumption. The University of Massachusetts Amherst has estimate that ML for one project can produce 284 tons of carbon dioxide, which is supposedly five

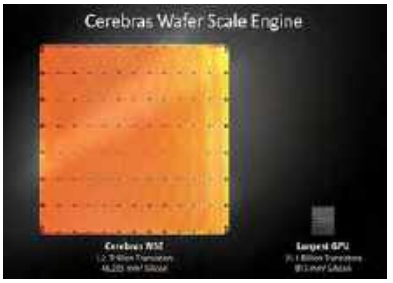

Figure 1: Cerebras ASIC chip (Source: Cerebras)

times worse for the environment than a car. The energy levels can be reduced by developing better learning programs or reduce the accuracy of the learning, but also by improving how the computer chips work by having the memory and the logic working closer or better together.

There has a been a great deal of work in the past few years on how to develop memories and processors that operate more like the

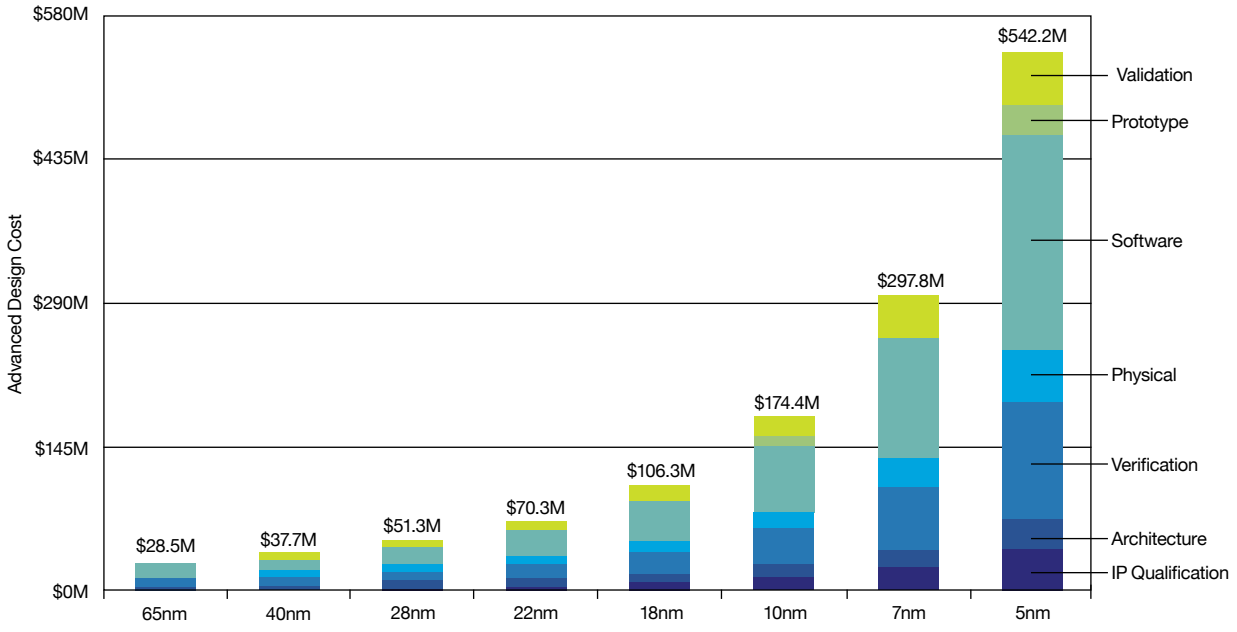

Figure 2: The rising cost of ASICs (Source: Handel Jones IBS)

human brain. GPU's in conjunction with CPU to help to process the data in a more parallel manner. FPGA's used to help off load some of the work load between the CPU and memory. Intel's Optane™ Memory used in a similar manner to cache memory from the DRAM so that the CPU can access it faster at lower energy. IMEC's IEDM paper uses an analog-in-memory computing process that can improve energy consumption by 10x over current technologies. However, until specific silicon solutions can be built to meet the demanding requirements of deep learning alternatives are needed.

ASICs: The Current Solution

Application specific integrated circuits (ASICs) have been emerging to specifically address deep learning. Google, and Amazon have both introduced silicon to address deep learning, and both are working with multiple entities to develop the software for different AI applications that utilize deep learning. Multiple AI chip startups are developing new technology. One receiving a great deal of press is Cerebras, who developed a nearly entire wafer ASIC chip using 28nm technology (Figure 1). One of the key issues with ASIC's is cost, the other is yield.

It is getting extremely expensive to develop, design, and manufacture ASICs. There is a good reason Cerebras used the 28nm technology node to produce their AI chip. It is 6x cheaper to produce an ASIC at 28nm than at 7nm (Figure 2). Intel, AMD and Nvidia are, or will be, producing AI chips at 7nm in 2020. There will be tradeoffs in cost versus performance of ASIC chips, compared to standardized chips such as central processing units (CPU) or graphics processing units (GPU). Intel has been developing neural network processors probably at 14nm, that are essentially ASICs, which could potentially outperform competitive ASICs due to the difference in transistor performance of 14nm over 28nm. Also, the operations per power of ASICs is currently too slow for many future edge compute solutions.

Chip yields are another issue, the ASICs being developed for AI have

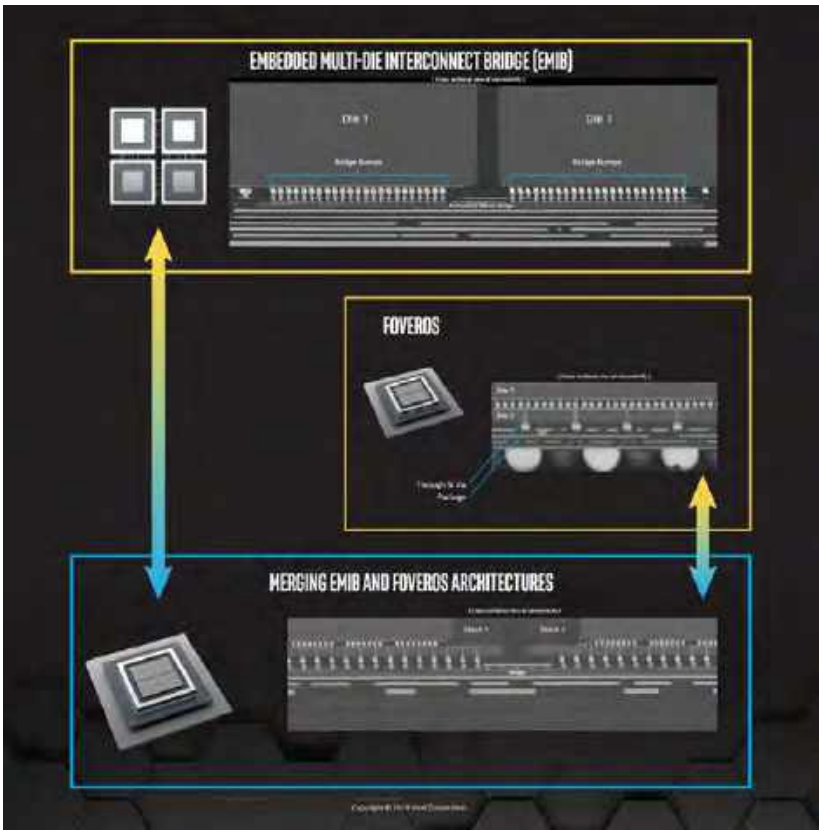

Figure 3: Advanced substrate and assembly capabilities at Intel enabling next generation product architectures. (Source: Intel)

a fairly large die size. The Cerebras chip is a case in point using most of a 300mm wafer, Cerebras has incorporated a significant amount of redundancy into their design which can help, but in the long run low yields add to the ASIC cost model.

Heterogenous Packaging an Alternative Solution

Heterogenous packaging provides an alternative to the AI ASIC chips, and the round peg into a square hole of both standalone CPU and GPU implementation into AI engines. The ability to package CPU, GPU, network neural processor (NNP), memory, analog, and accelerators into a single package makes it possible to reduce the short-term power consumption challenge that AI faces, but also improve the learning function by being able to use the optimum chip for that specific application for learning at the edge, and creating the ultimate system-in-a-package (SiP).

The ability to develop a heterogenous package was first attempted with through silicon vias (TSV), the concept being that memory, logic and other chips could be stacked on top of each other forming a SiP and shortening the interconnect length, thus improving system performance. Unfortunately, the heat generated by the chip stack caused performance issues. After many attempts to find ways to economically cool the TSV chips, heterogenous 3D IC development took another tack, with TSMC developing the chip-on-wafer-on-substrate (CoWoS). Using this process TSMC was able to develop SiPs that could combine multiple chips on the same package substrate, providing higher performance than interconnecting them on the printed circuit board (PCB). The technology has evolved to enable the chiplet revolution emerge in the market place where multiple large cores can be placed in the same package to realize a more powerful compute system.

Over this past summer, Intel released the combination of embedded multi-die interconnect bridge (EMIB) and Foveros 3D packaging technologies that together enable die-to-die communication using

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The Evolution of Advanced Packaging

By Swati Ramanathan, and Stephen Hiebert, KLA Corporation

The technical evolution of advanced wafer-level packaging is motivated by several drivers. First, the growth in packaging has accelerated as Moore's law appeared to slow down. Shrinking process nodes have long been a key component of Moore's law, but as advanced nodes hit an economic feasibility wall, progress in the front end slowed. This naturally shifts the focus of development to other areas like packaging, where improvements are still readily being realized.

Second, consider that demand for multifunctional devices, such as those powering the Internet of Things (IoT), is increasing. These multi-functional devices may include sensors, memory, and logic functions coming from separately manufactured components from varying process nodes. This drives the heterogenous integration of devices, i.e., the packaging and assembly of these devices into a single system.

Finally, the increased adoption of advanced computing artificial intelligence (AI) applications require chips with a high memory bandwidth. Today's rate-limiting step is not processing speed, but the speed at which data flows through interconnects in vertically stacked and laterally arranged schemes. In order to push data at high speeds and enable economy-in-power consumption and form factor, it is necessary to drive up the connection density between die stacks as seen in high bandwidth memory (HBM) and hybrid bonding schemes, or it is also possible to drive up the density of redistribution layers (RDL) with high density fan-out (HDFO) architectures, resulting in smaller features and finer pitches.

These three factors are responsible for increasing the criticality of packaging.

Toward Greater Value

Packaging has long been seen as the simplest part of the semiconductor manufacturing flow. Historically, process complexity was lower; however, the trends outlined above are bringing about a paradigm shift in packaging, and rapidly increasing its complexity and relative importance in the semiconductor value chain.

The challenge lies in advancing the packaging processes such as lithography, deposition, etch, die singulation, and reconstitution to keep pace with industry needs. The small feature sizes resulting from high interconnect and evolving RDL line and space densities place further demands on process tool capabilities and material complexity to make sure the process is robust. The number of process steps is vastly increased in new advanced packaging technologies. Yield excursions at this late stage in chip production are extremely costly, especially with 3D stacked schemes.

Increasing Yield in Packaging

Increasing yield has been a critical part of the success and scale of the semiconductor industry today. The cumulative effects of small yield improvements per process step are enormous, since they stack up exponentially. Since many complex processes involve a large number of process steps, yields of individual steps need to be at or close to 100% for the product to be viable.

The relatively straightforward flow in historical packaging methods meant that the requirement for

Continued on page 54

25 Years Perfecting the Art of Metrology

By Françoise von Trapp

I first met Dr. Thomas Fries, Founder and CEO of FRT, The Art of Metrology in 2016 at SEMI Europe's 3D Summit in Grenoble. Fries became a big fan of 3D InCites, following us on social media, and sharing our content. Over the next few years, Fries and the team at FRT became more involved in the 3D InCites community, providing valuable insight for our tech round-up blogs, participating in the 3D InCites Awards, and winning the 2017 Equipment Supplier of the Year Award for the MicroProf (Figure 1). In 2018, FRT became a 3D InCites banner advertiser. In 2019, we expanded our partnership to include FRT's sponsorship of Packaging IFTLE, Phil Garrou's blog, so that Phil could continue delivering his advanced packaging message to his followers. You see, this is how a community works.

Figure 1: The 3D InCites Award on display

In recognition for being a 3D InCites Community Leader, we selected FRT to be featured on the cover of the 2020 Yearbook. It's a happy coincidence that 2020 also happens to be the 25th Anniversary of the FRT brand. It seemed a good time to tell the whole FRT story.

The FRT Brand Story

The story of the FRT brand is a very personal one for Thomas Fries. In its first incarnation, the FRT brand stood for "Fries Racing Team", Fries' motorbike racing team, which he started in 1981. Since then, it has come to mean a number of different things.

In the second incarnation of the FRT brand, the letters stood for "Fries Research & Technology". After receiving a Ph.D. in Physics from the University of Bonn in Germany, Fries spent four years at Günther Systemtechnik GmbH building a department for scanning probe microscopy (SPM). SPM comprises scanning tunneling microscopy

Figure 2: First-generation MicroProf — tabletop version

(STM), atomic force microscopy (AFM) and other probing technologies to resolve surface details down to the atomic level. In 1995, Fries purchased all the SPM equipment from Günther Systemtechnik, and along with two co-workers, parlayed his passion for motorbikes into a contract lab offering SPM services to a variety of manufacturing industries. In addition to SPM, they offered additional analytical services such as time-of-flight mass spectrometry.

"From the beginning, we focused on customer needs, offering measurement services primarily for our customers in the automotive and medical markets," Fries recalls. If they didn't have the necessary equipment, they rented it from the nearby Max Planck Institute, he said.

In those early years, FRT focused on automotive, medical, optical, and electronics markets. The team saw a need for a high-resolution tool that could measure very small areas and would bridge the gap between meters and nanometers. What Fries envisioned, was a multisensory tool that could be used to measure all surface dimensions. He calls it "bridging the gap from meters to nanometers." In 1998, FRT's first generation multi-sensor tool was built, and the company evolved from being a service organization to an equipment supplier (Figure 2).

"We never intended to build and sell tools, we just wanted them to use internally," says Fries (Figure 3). "But then we realized developing a tool and scaling it was more interesting than doing high knowledge services."

For the next eight years, FRT found its niche, developing and rolling out the second-generation multi-sensor tool, and continuing to target the automotive and optics, machining engineering and electronics markets, while also maintaining the contract business.

In 2006, as more pioneers of optical metrology entered the optics space, keeping prices low, Fries made the decision to break into the semiconductor market, as this space was being avoided by other players due, in part, to long turnaround times. In Fries' opinion, the semiconductor industry offered an open playing field (Figure 4).

"This was an opportunity to differentiate our company from the other players, and be unique by focusing on more complex technologies," explained Fries. "Sure, it was risky, but there's no fun without risk!"

To get started, FRT developed brand-new multi sensor tools for

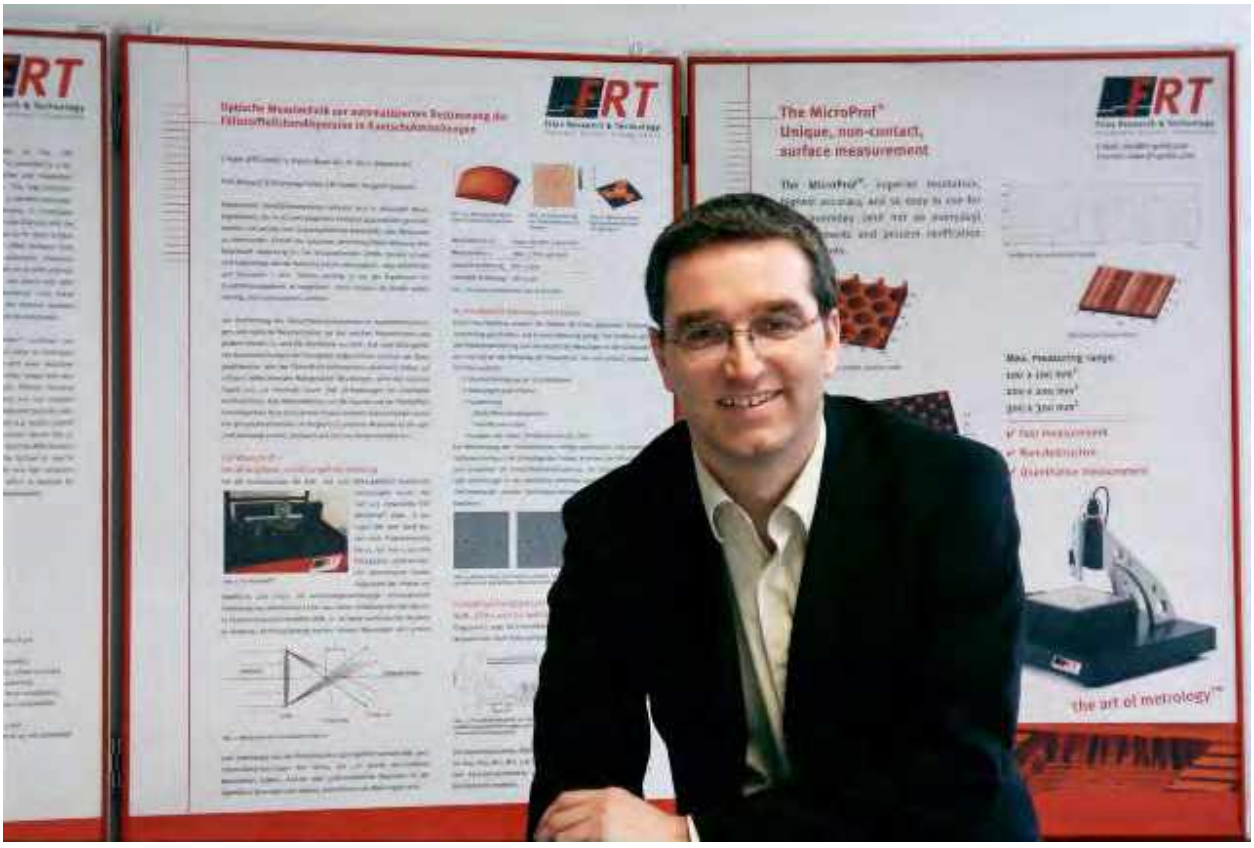


Figure 3: Thomas Fries, in the early days of FRT

Figure 4: FRT showcasing its services at a trade show in 2006

the fab. In-house software developers wrote the interface themselves. As they were doing this, the LED industry was ramping up, and with it came a need to measure total thickness variation (TTV) of materials and exotic substrates. This called for a high-speed, high resolution, very accurate optical system, and FRT delivered. It quickly grabbed 100% market coverage of sapphire wafer metrology in Taiwan and 40% in China. It also served the traditional semiconductor and MEMS markets, but the market share was still small.

The crash of the LED market in 2011 came just as FRT had taken the step from R&D tools to production with fully automated tools in the LED market (Figure 5). As a result, 2012-2014 was a period of struggle for FRT's sales organization, says Fries. But the company persevered and continued to develop fully automated third-generation metrology tools with a wafer handling system within an Equipment Front End Module (EFEM) for the semiconductor and MEMS markets. By 2015, it had recovered thanks to traction in its original markets: automotive and optical, and big European customers.

FRT: The Art of Metrology

2016 brought the third incarnation of the FRT brand: FRT, The Art of Metrology, along with new assets and a logo change. 80% of its tools were being sold in the semiconductor and MEMS spaces. The company also broke into the advanced packaging market, succeeding with top-tier integrated device manufacturers (IDMs) and memory makers in the USA and Asia.

With the new brand came an enhanced idea about marketing, as well as a change in attitude about metrology. The company focused

Figure 5: (left: current MHU / right: older version) metrology tool with Material Handling unit MicroProf® MHU

on its nimbleness and flexibility. When working with customers, Fries and the whole FRT team took a holistic approach, examining each project from the point of view of the customer, and investing in new technology development (Figure 6).

"From 2016-2019, FRT was one of the companies with the highest annual growth rate," said Fries. "It became clear that if we were going to continue on this trajectory, we needed a strategy." Part of this was to create a demo facility and open a new subsidiary, FRT of Taiwan. But expanding a global footprint very fast can be difficult for a small company. Multiple advanced orders can create a cash flow crunch. It was time to consider other options.

FRT: A FormFactor Company

In what can only be described as one of the fastest mergers in recent semiconductor history, in November 2019, FRT was acquired by FormFactor in a simultaneous signing and closing. As part of the deal, FRT will maintain using its well-established brand, and operate as a FormFactor company.

Ten years ago, FormFactor was primarily a DRAM probe card provider, with a very concentrated and volatile demand profile. In 2012, the company began to diversify by acquiring MicroProbe, the number one supplier of advanced non-memory probe cards, to expand its presence in the foundry and logic markets. In 2016, the company acquired Cascade Microtech, which brought RF probe cards and engineering systems. With the FRT acquisition, the goal was to expand FormFactor's reach into optical metrology focused on the advanced packaging space, explained Mike Slessor, CEO, FormFactor (Figure 7).

"Advanced packaging is driving our business," said Slessor, "This is a growth area in the industry, and we are dedicating more resources to roadmap innovation in serving advanced packaging applications."

Slessor, Fries, and Amy Leong, CMO and VP of M&A for FormFactor all agree that the two companies are a natural fit. FormFactor

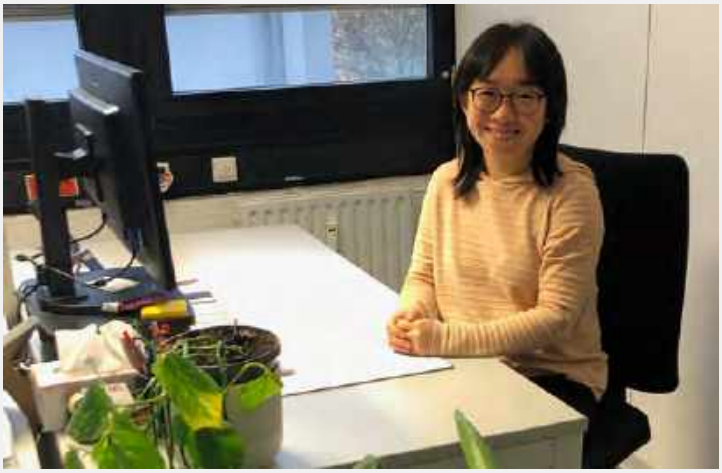
The People of FRT

While visiting FRT's headquarters in BergischGladbach, I met members of the staff and talked with them about their roles, and what sets FRT apart. Here's what some of them shared.

Alejandro AvellanHampe, CTO, has been with FRT since 2014. An electrical engineer, he got his start in the semiconductor industry at Infineon, working on different types of sensors. At FRT he guides the applications, software and assembly teams, providing input for developing customized solutions, which he explained is a key differentiator for FRT.

Michael Ulbrich, Sales Manager in Europe for all English speaking countries joined FRT in 2017 after a long career as an engineer for optical communications, during which he held various leadership positions in project management and technical sales for the automation and telecommunications markets. At FRT, he provides technical consulting and solutions for shaping the tool to customer needs. "The added advantage our multi-sensor tool offers our customers over our competitors, is its ability to have sensors and functions added to it in the field," he explained.

The People of FRT



Kuang Wang, sales engineer for Asia-Pacific, is also the resident plant sitter for colleagues who are out of the office. She joined the team in March 2018. Originally from China, she holds a master's degree in microsystems and microelectronics from at the University in Chemnitz. Based in BergischGladbach, at FRT's headquarters, she manages a small team based in Asia, providing technical conversions and coordinating needs of customers in Asia markets.

Corinna Meyer joined the team in January, 2018. She manages back office sales, analyzing statistics and forecasting future sales. She also serves as a direct contact for customers when customer service is not available. Almost two years in, she declares FRT is a "Good place to work."

Patrick Voos is a relative newcomer to FRT, joining in October of 2018. He is responsible for FRT America team, and supports sales focused in the Americas market. He also develops strategies to support Fries. Prior to joining FRT, Voos worked for 15 years as a materials scientist for a US company that specialized in metallographic materials. He made the leap from scientist to sales at FRT, learning sales, marketing and product development on the fly.

is a leader in electrical test for the semiconductor and advanced packaging industry, while FRT's core competencies are optical metrology and inspection.

"FRT has great technology with good adoption, but to be a world class supplier, you need the infrastructure and ability to support it globally. As a small company, it's not easy to grow that organically because it's expensive to build that infrastructure; but it's an infrastructure and set of customer relationships that FormFactor already has," said Slessor.

"We wanted to have a global footprint but lacked the resources to hire and do more development," Fries explained. "This is the best situation, because FormFactor is not active in the optical metrology business. All others (competitors) would have squeezed us out, and that would have been the end of FRT. Now, we are a new business unit. We have the chance to perform. They want to build up the FRT business."

"We took a broad look at the metrology players, and for a variety of reasons, FRT bubbled up," explained Leong. "The transition was easy because there was no overlap in technology offerings." FRT's focus on metrology and inspection for advanced packaging and niche applications such as silicon photonics was a key selling point, explained Leong. Others included size, scale, and customer engagements, including customer pull for hybrid solutions. (In a happy coincidence, Leong says she first learned about FRT as a company from their presence on 3D InCites.)

The Next Era

January 2020 kicked off a new era for FRT as the company added defect inspection tools for wafer applications to its portfolio. This new capability was customer driven, said Fries. A customer had a need, and FRT developed the capability.

The modular system is capable of defect inspection down to one micron. It uses image sensing technology to find scratches and particles in wafer samples and

Figure 6: The Wall of Fame at FRT Headquarters

then uses metrology to analyze the defect to see if it is a latent or killer defect. It performs full wafer mapping and different types of inspection.

By first looking for rough defects and then only zeroing in on trouble spots with 3D metrology, throughput is increased, explained Fries. The idea is to identify "golden die" and compare it to those with defects.

Customers will be able to order either full inspection systems or combine both metrology and inspection into one tool. Integrating both capabilities into one platform allows for the same software that are components to be used on all tools.

"This offering is unique to FRT. We are the only manufacturer on the market that provides these capabilities in a single platform," said Fries. "Others have different platforms for inspection and metrology."

The FRT Culture

After spending a day at FRT's headquarters near Cologne, Germany, and meeting members of the team from the executive management to administrative support, it's easy to see what makes it such a great place to work. The company fosters a diverse and inclusive workplace, with employee representation from 17 different countries of origin. 33% of the workforce are women, staff is between the ages of 23 and 60 years. The young people bring in new ideas, and the older employees mentor them. In this way, they learn from each other (see sidebar).

In addition to hosting a summer barbeque and Christmas party,

Lars Vitense celebrated 2 years at FRT in November 2019. He focuses on semiconductor sales for Germany, Austria and Switzerland. He says he's not a complete nerd: "My degree is in laser science physical engineering, not just physics." He says his technical background is essential to his role. "We have to understand business, but in our market, it's important to understand the technical questions," he explained. "You don't want to say "yes" automatically to customer requests." Rather, the sales team works closely with the applications department to see if requests are possible.

there is FRT Day, a team building event featuring activities and sports. Community outreach includes offering training to primary school teachers along with materials to help teach physics and science to children. Lastly, the company hosts a Technology Night during which they open their doors to the community from 6pm to midnight so people can come and learn about what they do. This gives students the opportunity to see where they could work someday, explained Sarah Trompetter, FRT's marketing and communications manager.

Dr. Jürgen Koglin, head of applications at FRT, says that from teh start, the company has had a family-like atmosphere. "We were a small family at the start. Now we're a big family," he says. Koglin joined in 1997, just as FRT was getting started. He knew Fries from his time as his student at the University of Bonn. After receiving his PhD in Physics from University of Muenster, he joined the company as employee #7. As a result, he was very involved in company decisions. "Everyone was involved in the beginning," he recalls.

All tool development at FRT is application centered. While they begin with standard tools, the last 5-10% is custom configured. Koglin and his team of five work with customers to perform test measurements and feasibility studies on customer samples to determine what type of sensor, measurement and instrument is suitable for the customers tasks. While the work is technical, the team works closely with the sales team to ensure they recommend the best combination to the customer.

Koglin says that over the years as they work on more intricate technologies, the solutions become more complex. There are many types of applications that must be solved with one tool and different sensor types, but that's what keeps his job so interesting.

As a department head, Koglin gets to build his own team. He says he looks for motivated people who can think on their own and develop solutions, but also work well on a team, as all projects require collaboration. "It takes about a year to become involved in the techniques," he said. "So we look for people who will stay at least 3-5 years."

Bastian Tröger, product management, is another FRT veteran who came to the company straight from academia. Armed with his master's thesis, in which he constructed a tool for measuring diffraction efficiency, he joined FRT in 2007 as part of the development team and worked his way to product management. He's been a team leader in PM since 2017.

Tröger reminisced about his days in the cleanroom and how exciting it was as new products were developed. Today his main focus is on typical product management tasks. But he also enjoys working with the field engineers, supporting on-site tool acceptance and application development at customer facilities.

What has kept him here for more than a decade? "If you work here, it's not a routine job. It's different every day and there are always new challenges," he said. "We've got a good, collaborative team and we know each other well."

What's Next for FRT?

25 years is a good chunk of time in an industry that is barely over 50 years old. In that time, FRT has established a strong foothold in process control for heterogeneous integration technologies. Going forward, as device reliability becomes more and more critical, FormFactor will provide the muscle to take this nimble player to the next level without sacrificing its flexibility, integrity, or company culture. I'm excited to see what the next quarter century has in store.

Figure 4: FRT showcasing its services at a trade show in 2006

The People of FRT

Mate Raczka joined FRT in August 2019, working in a newly created position supporting custom tool orders. His job is to define suppliers for hardware items.

And last but most importantly, I spent the day with **Sarah Trompetter, FRT's marketing manager**. She joined the team last year and is responsible for maintaining and promoting the brand and company culture.

FRT's software is developed completely in-house by this team of software engineers.

In the Production Unit, I met **Gaurav Ravva, Project Manager**, who walked me through ongoing projects. In semiconductor manufacturing, companies each have their own challenges, he explained. In coordination with the software and application departments, it's his job to optimize the tool to the needs of the customer integrating multiple sensors on the same tool and making sure it can support different applications for the sub-micrometer measurement ranges.

Marketing and product management work closely together.

The IT team helps even with the smallest computer problems.

How AiP Technology Helps Enable 5G and More

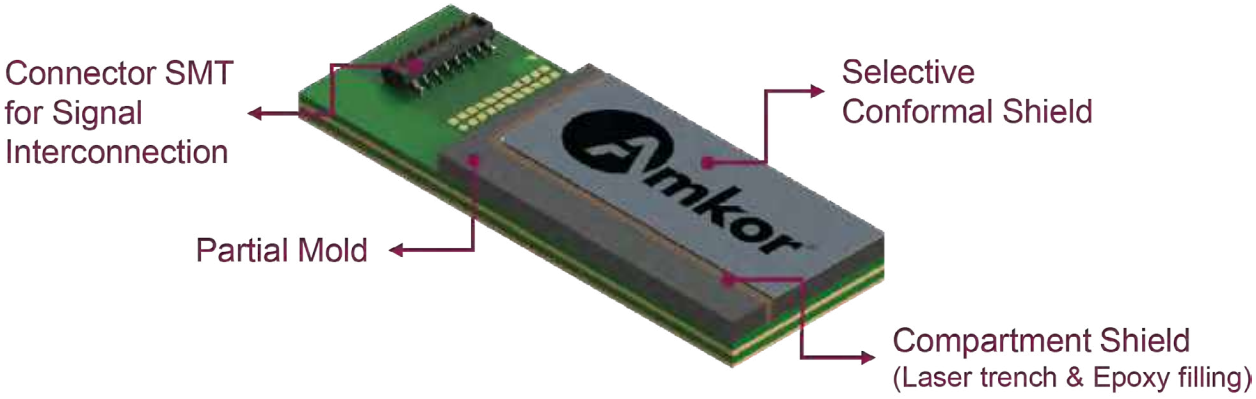


Figure 1: A look inside Amkor's AIP solution.

By Vik Chaudhry and Curtis Zwenger, Amkor Technology, Inc.

For 5G smartphones and other millimeter wave (mmWave) applications, antenna integration, either through antenna in package (AiP) or antenna on package (AoP) technologies, simplifies the challenges associated with designing products that operate at these high frequencies. A variety of AiP/AoP design methodologies provide the required form, fit, and function for these applications and can include more than one antenna or an antenna array. Today's AiP/AoP technologies can be implemented through standard as well as custom system-in-package (SiP) modules to achieve a complete radio frequency (RF) front-end (RFFE) subsystem.

Projected Growth for 5G, mmWave and RFFE Modules

In mmWave applications, signal loss becomes critical and the design challenges increase in complexity. In addition to emerging 5G smartphones, other applications that operate at very high frequencies and demand a small size include wearables, small cells, security cameras, radar units in autonomous vehicles, and numerous Internet of Things (IoT) wireless nodes. By 2023 over 1 billion mmWave units will be produced annually according to Gartner market research. With AiP technology, the antenna is no longer a separate component within the wireless device, but is integrated in a SiP with RF switches, filters, and amplifiers. According to consulting firm Yole Développement, the total RFFE module SiP market is projected to reach US $5.3 billion by 2023, representing an 11.3% compound annual growth rate (CAGR).

AiP/AoP at Amkor

Instead of separate RF system on chip (SoC), baseband (BB) SoC, surface mount technology (SMT) matching circuits, and a discrete antenna, today's fully integrated RF front-end module is completely achieved with AiP technology in SiP. In addition to a reduced size required for handheld and other small mmWave devices, AiP/AoP provides improved signal integrity with reduced signal attenuation and addresses the range and propagation challenges that occur at higher frequencies. As a leading outsourced semiconductor assembly and test (OSAT) supplier, Amkor has pioneered the packaging technologies required for RFEE subsystems (Figure 1).

Implementing AiP/AoP Technologies

Depending on the frequency range, different platforms are used for both the antenna and the IC package. In addition to AiP, the integrated antenna can be mounted on the package (AoP), or on a substrate (AoS), or in a SiP mmWave antenna module and the AiP approach itself can vary from package to package. For applications below 6 GHz, a flip chip ball grid array (FCBGA) or double-sided ball grid array (DSBGA) are two possibilities. For applications in the 28 GHz to 39 GHz range, the antenna could be a SiP module antenna or a flip-chip chip-scale package (fcCSP) with package-on-package (PoP) antenna. Applications in the 60 to 77 GHz range benefit from a wafer level or low-density fan-out (LDFO) package to the most advanced high-density fan-out (HDFO) packaging.

RF shielding techniques include dual-side mold, conformal shield, compartment shield using laser trench and paste filling technology, partial molding, selective conformal shielding, and hybrid SiP designs. These techniques implement a variety of materials to conductive lids as well as cored, coreless, and low coefficient of thermal expansion (CTE) and conformal shielding materials.

Packaging technologies for AiP/AoP include:

- Body sizes up to 23.0 mm x 6.0 mm with several smaller options
- Up to 14 substrate layers
- Thin-film redistribution layer (RDL) and dielectrics for 77 GHz and higher applications

With Amkor AiP/AoP technologies, system designers get:

Continued on page 56

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Temporary Bonding and Mold Process to Enable Next-Gen FOWLP

By Arnita Podpod and Eric Beyne, imec

Temporary wafer bonding processes were initially developed for enabling three-dimensional (3D) stacked integrated circuits (ICs). For example, dies can be stacked on top of each other using die-to-wafer stacking to create 3D IC stacks. Through-Si vias (TSVs) and microbumps are used to interconnect the finished dies. These techniques require the processing and handling of ultra-thin substrates, which has been enabled by the first-generation of temporary wafer bonding solutions. By using these technologies, the thinned device wafers on a carrier can now be processed through successive multiple backside process steps. At the end of these processes, wafer de-bonding solutions allow the carrier to be separated from the device substrates with only a minimum of stress.

However, recent advancements in assembly and packaging brought along new challenges for temporary bonding. An example is the rise of fan-out wafer-level packaging (FOWLP), a flavor of wafer-level packaging (WLP) technology that answers the demand for more functionality, increased I/O count, smaller form factor and cost reduction. With FOWLP, a redistribution layer (RDL) is created to re-route the die connections (I/Os) to the desired (bump) location on top of the die surface. The RDL is created either prior to or after a wafer over-molding step. The function of the epoxy mold is to protect the individual components and hold them all together.

The processing of these reconstructed over-molded substrates is putting new constraints on temporary bonding. One of the main challenges is stress holding, related to the large mechanical property mismatch between the over-molded substrate and the carrier. Temporary adhesive solutions must now cope with high and varying stress levels throughout the various process steps, while trying to maintain the wafer geometry (i.e., warp and bow).

Meeting the Requirements of a Novel FOWLP Technique

In this article, we introduce advanced molding materials and new temporary bonding and de-bonding solutions. These solutions have been developed to answer the needs of a new flavor of FOWLP developed at imec — its flip-chip on fan-out wafer-level packaging (Figure1). More specifically, the challenge was to realize extremely low die shift in combination with low wafer bow and warpage — after wafer over-molding.

Although specifically developed for this new FOWLP flavor, the technology may open new horizons for the processing of over-molded substrates. For example, if low-warpage can be achieved, these overmolded substrates can access more standard silicon back-end-of-line process equipment, eliminating the need for dedicated toolsets that can handle large wafer bow.

Prior to giving more details on the

Figure 1: Concept of the flip-chip on fan-out wafer-level package.

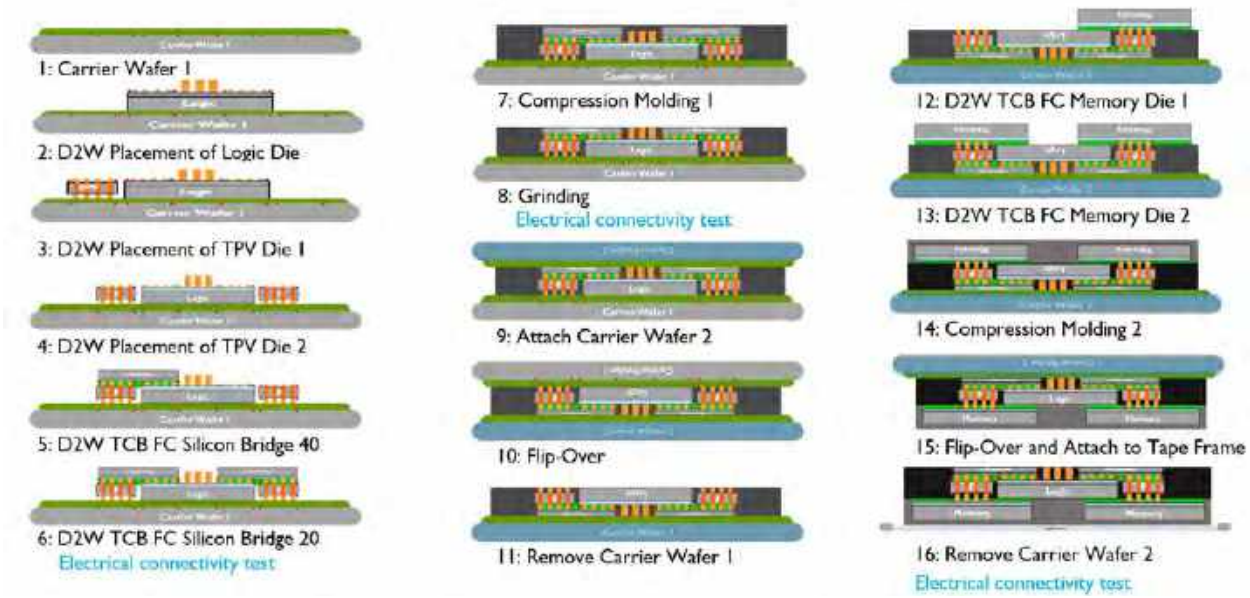


Figure 2: Flip-chip on FOWLP: assembly process flow.

new molding and de-bonding technologies, we will briefly summarize the major steps of the flip-chip on FOWLP technology — as these have set the requirements for the new technology.

Flip-chip on FOWLP: A Quick Summary

Imec's flip-chip FOWLP technology was developed to push the boundaries of conventional FOWLP solutions in terms of chip-to-chip connection density. Using this FOWLP approach on 300mm wafers, ultrahigh interconnect density with 20µm pitch are now within reach. The technology is particularly attractive for mobile applications as it enables a cost-effective wide I/O memory-to-logic interconnect in a very small form factor. But it may also become an enabling technology for heterogeneous integration targeting high-performance applications.

Flip-chip on FOWLP basically uses a mold-first approach: dies are first assembled on a temporary carrier, followed by wafer over-molding. In a final stage, the redistribution layer is created, and connections are made. But contrary to standard mold-first approaches, dies are now over-molded after the formation of the chip-to-chip interconnections. This way, chips are already interconnected before being shifted during the over-molding process.

The imec team demonstrated the feasibility of this approach by using a test vehicle that is composed of seven individual (dummy) chip components: wide I/O DRAM, Flash memory, logic, two through-package vias, and two Si bridges. The interconnecting Si bridges and the through-package via chips are key components to realize the high-density connections. Through-package via chips are Si dies with through-Si vias (TSVs) and bumps of 40µm pitch. The Si bridges have bumps of 40µm and 20µm pitch. These components form a bridge between the functional dies (e.g. the logic and memory dies), enabling ultrahigh chip-to-chip interconnect densities with 20µm bump pitch.

In a first step of the flip-chip on FOWLP assembly process flow (Figure 2), the through-package via and logic dies are placed on a carrier wafer with a temporary bonding layer on top. Next, the Si bridge (with 40µm and 20µm bump pitches) is attached using a thermocompression bonding (TCB) step. In this process step, bumps with 40µm pitch are attached to the through-package via side and to the left side of the logic die. The 20µm pitch bumps are attached to the right side of the logic die. In a next step, the wafer is over-molded by a liquid mold compound. Afterwards, the Cu pillars are exposed through grinding so that later, they can connect with the RDL. After flipping the thinned wafer to a second carrier and removal of the first carrier, the memory dies are assembled using flip-chip technology. A second wafer-level molding and removal of the second carrier complete the process flow. The result is a complete package of only 300-400µm thickness (excluding the solder balls).

Finding the Right Adhesive and Mold Materials

Throughout the assembly flow, two temporary carrier substrates are being used. Their role in the assembly process puts very specific requirements on the adhesive material that is used for temporary bonding, and on the release material used for de-bonding.

The main role of the first carrier system is to assemble chips (i.e., the through-package via and logic dies) with extremely high inter-die alignment precision: +/- 3µm die-to-carrier placement accuracy is needed to allow for 20µm bump pitches. Such an accurate placement can be obtained by incorporating alignment marks into the carrier and die designs. The first adhesive material must therefore be sufficiently transparent to enable pattern recognition for alignment.

Next, the imec team looked for a material that allows the dies to be placed at room temperature. At this temperature, thermal expansion issues can be eliminated, enabling more precise die-to-carrier alignment. At the same time, the adhesive must be able to withstand higher temperatures during a subsequent TCB die-to-wafer bonding step (see steps 5 and 6 in Figure 2), and the material must be capable of maintaining the dies in place during the wafer over-molding step. In the end, the adhesive material should also allow carrier-one debonding while maintaining minimum wafer bow.

The main role of the second carrier is to enable the removal of the first carrier system. When this is removed, the front-side of the original devices can be re-accessed for testing and further processing. A major requirement for this second carrier system is, therefore, to enable the selective removal of the first carrier, without damaging the reconstructed wafer or increasing warpage.

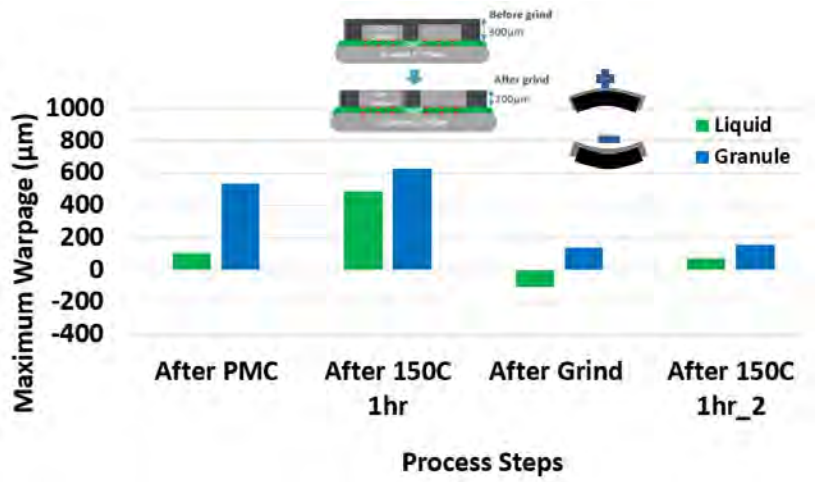


Figure 3: Warpage evolution at different process steps with liquid (green) and granule (blue) type of molds. Warpage remained low during succeeding process steps.

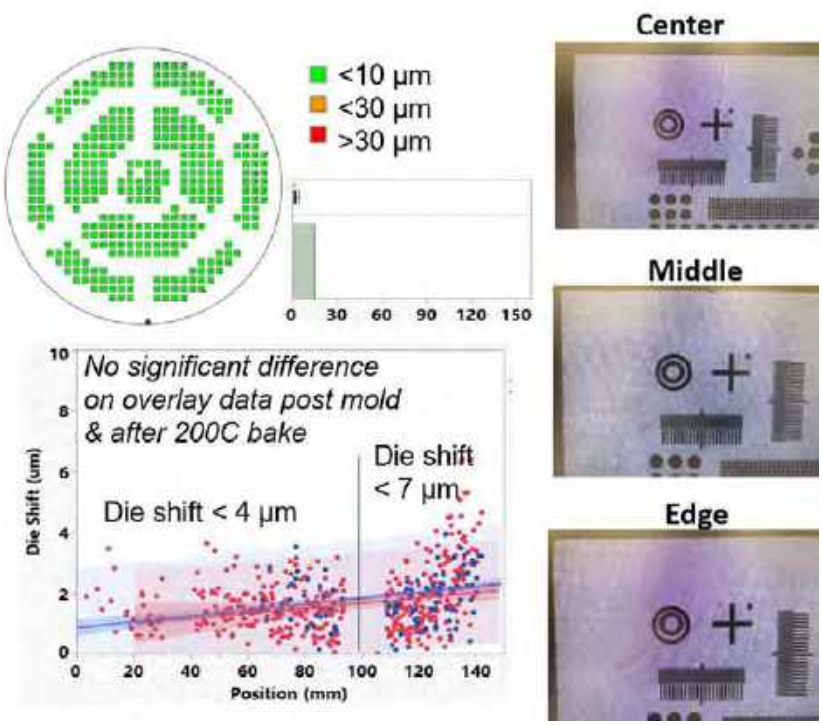


Figure 4: Die-to-carrier overlay, post-mold and post-bake, with the liquid mold material. The results show that post-die shift did not change after subjecting the molded wafer to 200°C for two hours — supported by the circle-in-circle images of a die from center, middle and edge of the wafer. A similar result is obtained for the granular mold material.

Die shift, wafer warpage and bow can also be influenced by the mold material and wafer over-molding techniques. The assembly flow for the flip-chip on FOWLP involves two separate mold steps. A first over-molding step takes place after the silicon bridge is placed; a second after the memory die is flip-chip attached. It will be key to identify the right combination of temporary bonding and mold materials and processes to guarantee a low wafer distortion and die shift after molding.

The Outcome: Record Low Die Shift and Wafer Warpage

The team set up several experiments to evaluate different carrier systems, temporary adhesives and mold materials. In partnership with Brewer Science Inc., a new temporary bonding material for room temperature die bonding was introduced, referred to as BrewerBOND® C1301. Both liquid and granular forms of advanced mold materials (referred to as M1 and M2) have been explored. The impact of these materials and processes on die placement, die shift, and wafer geometry was investigated (Figure 3).

On blanket wafers, the granule mold material in combination with the temporary bonding material shows more stability than the liquid one when exposed to different temperatures. This can be explained by the higher glass transition temperature of granular vs. liquid mold materials.

On molded wafers with exposed embedded dies, the combination of a silicon carrier with the new temporary adhesive and advanced mold materials results in less than 2µm die-to-carrier mismatch, even after exposure to temperatures of 200°C for 2 hours — for both granular and liquid molds (Figure 4). An extremely low warpage of less than 200µm was achieved on the full 300mm wafer. These values are way below the ones reported in literature.

The team also explored ways to efficiently de-bond the two carrier systems and remove the adhesive material. For the removal of carrier

one, a mechanical de-bonding technique was used that did not affect the second bonding. The use of a mechanical-de-bondable silicon substrate was preferred, as it was compatible with the initial requirement of having alignment marks on the carrier substrate. For carrier two, a laser-assisted de-bonding was chosen for throughput and productivity reasons. Successful selective carrier de-bond has been demonstrated (Figure 5).

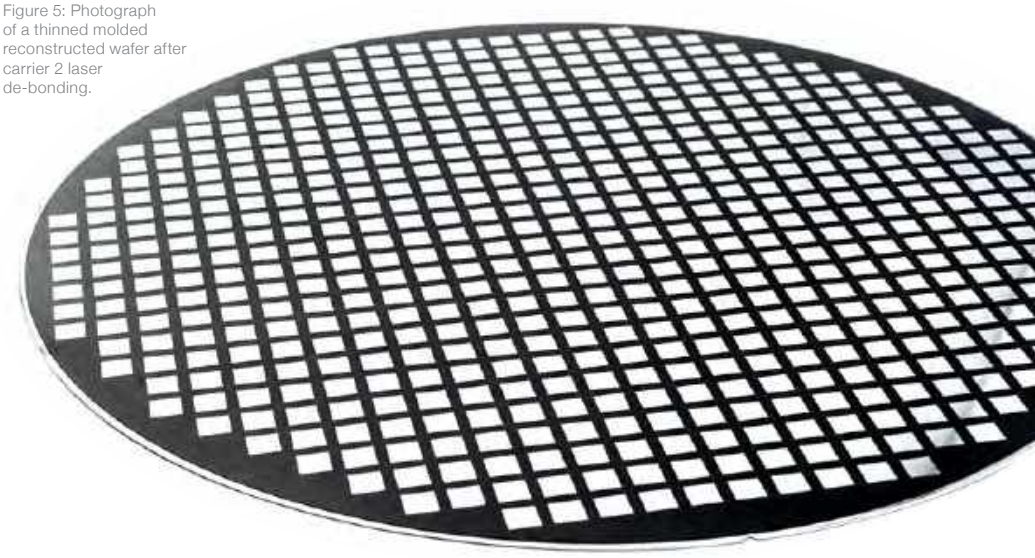


Figure 5: Photograph of a thinned molded reconstructed wafer after carrier 2 laser de-bonding.

Conclusion

Warpage and die shift are two main challenges when processing molded substrates. The results presented in this study show that the combination of a new temporary bonding material with two different mold material types on a silicon substrate can address these challenges. A quasi-zero post-mold die shift and less than 200µm warpage could be demonstrated.

The new temporary carrier technology is a key enabler for imec's flip-chip on FOWLP. But the importance of the results goes beyond that. First, the achievement of such a very low warpage enables the processing of over-molded substrates in standard silicon equipment. Second, the results open a different avenue for the FOWLP processing approach in general. For example, fine-pitch redistribution layers in combination with chip-first approaches will now become possible.

This low-warpage temporary bonding and mold process for 3D die-to-wafer assembly was the recipient of the 2019 3DInCites Process of the Year Award.

Hidden Figures: 3D X-ray Digital Cross Sectioning for Inspection and Measurement of Buried Package Interconnects

By Thomas Gregorich, Edith Hu and Masako Terada, ZEISS Process Control Solutions

Much has been written about the end of Dennard Scaling, the slow-down of Moore's Law and the impact that these events will have on future semiconductor performance and technologies. Much has also been written about semiconductor performance improvements that advanced IC packages are expected to provide that previously resulted from silicon scaling. However, these packaging improvements depend on one primary factor — the ability to shrink package-level interconnect size and density on a scale that has never been done before.

Although package technologies have evolved significantly since dual in-line and C4 flip chip packages were developed, minimum package interconnect feature sizes have not scaled significantly over the past 40 years. Just to put this into perspective, minimum silicon critical dimensions have scaled by nearly 10,000:1 during this period while minimum package interconnect size has scaled by less than 10:1.

The ability to scale package interconnects is in turn dependent on two factors:

- The ability of the manufacturing processes to fabricate the desired interconnect structures while maintaining acceptable levels of quality and process variation
- The ability to accurately set up and monitor the results of these manufacturing processes in a timely manner

While it is beyond the scope of this article to assess the viability of the various package manufacturing processes to fabricate the desired structures, manufacturing process setup and results monitoring are separate and equally challenging requirements and are the subject of this work.

Except for wire bonds, most internal package interconnects cannot be viewed either during or after the assembly process. As a result, physical cross sections are often the only available method for verifying the internal results of process setups and production builds. However, physical cross sections are destructive, take a long time to process, provide a limited field-of-view, are limited to two dimensions and are highly operator-dependent.

Fortunately, an innovative, non-destructive alternative to physical cross sections is available called "digital cross sectioning". Digital cross sections can replace most physical cross sections used for assembly process setup and construction analysis and can also be used in circumstances where products are "blind-built" without physical verification.

Digital cross section technology is available from ZEISS with the RepScan® system, which is based on the company's Versa 3D X-ray microscope with Resolution at a Distance™ and spatial resolution of 1µm at 50mm working distance, along with additional custom hardware and software as shown in Figure 1. The RepScan system can image and measure the following package features:

- Interconnect bond line and die tilt
- Bump-to-pad and through silicon via (TSV)-to-bump alignment
- Solder fillet extrusion, solder volume, and solder wetting
- Internal layer warpage and other X-ray imageable features

In the following sections we will demonstrate process setup and construction analysis data that was extracted non-destructively from a fully assembled 2.5D package using this digital cross sectioning system.

A typical 2.5D package consists of four high bandwidth memory (HBM) cubes and a central processing unit (CPU) mounted on a silicon interposer, which is in turn mounted on an organic substrate:

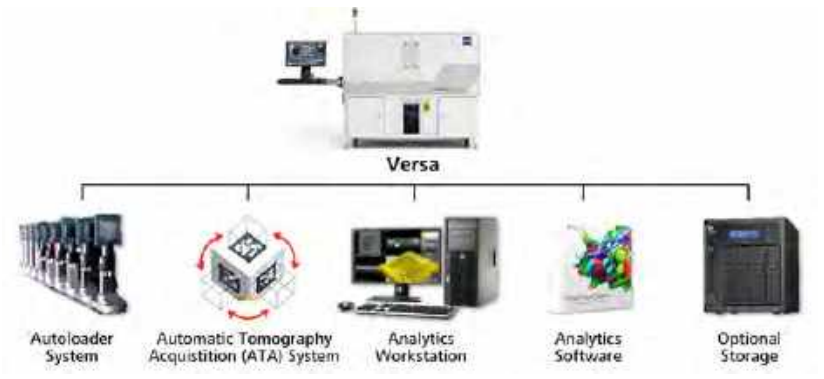
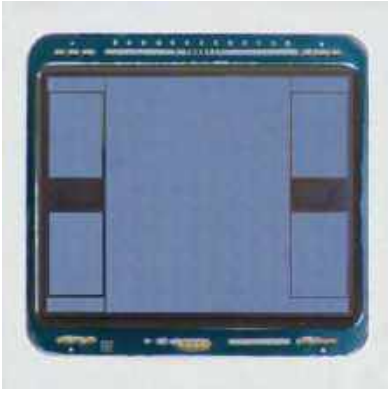


Figure 1: ZEISS Versa RepScan system.

- HBM cube – Consists of four to eight memory chips assembled on a logic chip and electrically connected using TSVs and micro-bumps. The HBM cube is a purchased part and is almost always assembled and tested in a different factory from the 2.5D package.
- 2.5D interposer – The process flow referenced in this article utilizes pre-stacking of the HBM and CPU on the 2.5D interposer before assembly to the organic substrate. The pre-stacked system is encapsulated with resin before being assembled on the substrate. An alternative assembly flow is to assemble the 2.5D interposer to the organic substrate before connecting the chips.
- Organic substrate – The pre-stacked 2.5D chip module is then assembled to the organic substrate using C4-type bumps and underfilled. Decoupling capacitors, stiffener rings, and heat spreaders might also be assembled on the substrate, depending on the application.



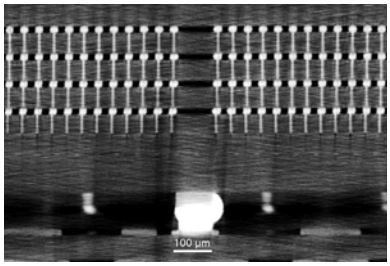
2.5D Package Features	
Body Size	55 x 55 mm
Body Height	2.8 mm
Substrate Thickness	2.0 mm
BGA Ball Pitch	1.0 mm linear
Number of HBM Cubes	Four
Decoupling Caps	Yes
Stiffener Ring	Yes

Figure 2: Image and overview of the 2.5D package used in this analysis.

The 2.5D package used in this analysis is typical of many current designs and is shown in Figure 2.

As previously mentioned, the HBM cube is a purchased part for the 2.5D manufacturer. While the external electrical interface to the HBM cube and overall stack height are defined by a JEDEC specification, the horizontal stack outline, internal electrical interconnects, and stack configuration are unique to each memory supplier. While it is relatively uncommon for a 2.5D customer to do construction analysis of an HBM cube, we have included this analysis to demonstrate the capabilities of the RepScan 3D X-ray digital cross sectioning system.

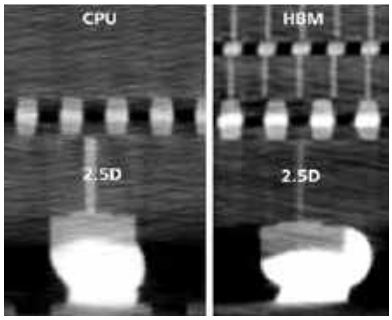
Because of the thinness of the memory chips and the small size of the micro-bumps, thermo-compression bonding is almost always used for HBM assembly. Figure 3 shows an image and a small sample of the characterization data that can be extracted from the HBM stack using the digital cross sectioning technique.



HBM Digital Cross Section Measurements	
Nominal HBM Bond Line Thickness	14 µm
Nominal HBM Die Thickness	54 µm
Nominal HBM Die Tilt	<1°
Maximum HBM Solder Extrusion	3 µm

Figure 3: Digital cross section view of HBM stack and critical dimensions extracted from Versa XRM 3D dataset

The assembly flow for this package uses pre-stacking of the HBM modules and CPU on the 2.5D interposer prior to assembly on the organic substrate. The pre-stacked chip set and 2.5D interposer are encapsulated and bumped before being assembled onto the organic substrate. Figure 4 shows images and a small sample of the characterization data that can be extracted from the pre-stacked chip set using the digital cross sectioning technique.



2.5D Digital Cross Section Measurements	
Nominal CPU-2.5D Bond Line Thickness	12 µm
Nominal HBM-2.5D Bond Line Thickness	15 µm
Nominal 2.5D-substrate Bond Line	58 µm
Maximum 2.5D Pad Mis-alignment	30 µm

Figure 4: Digital cross section view of 2.5D interconnects and critical dimensions extracted from Versa XRM 3D dataset

After encapsulation and C4 bumping, the pre-stacked 2.5D chip module is singulated and assembled to the organic substrate using mass reflow and then underfilled. Decoupling capacitors, stiffener rings, and heat spreaders might be assembled to the substrate at this time as well. At this point, the 2.5D package is complete and ready for electrical testing. Figure 5 shows a 3D rendering of the interconnects in the finished 2.5D package.

Figure 5: 3D rendering of all the internal interconnects extracted from Versa XRM 3D dataset showing the hierarchy and complexity of package interconnect.

Conclusion

In this analysis we have demonstrated a small fraction of the measurements that can be extracted from a fully-assembled 2.5D package using the digital cross section technique. Image quality and measurement results would be improved significantly if the technique were used when the package is partially assembled.

2019-2020: A Year of Contrasts Vs. A Year of Innovation & Growth

By Rozalia Beica, Industry Expert

When Francoise reached out to me to write this article, I thought it would be a great opportunity to review my 2019 experience and look ahead at what 2020 will bring.

A Year of Perseverance

2019 found the industry being strongly impacted by market trends, with an even stronger and downturn evolution observed last year for many companies -— but not all. The downturn was a result of various factors: from the typical cyclicality of this industry due to capacity, inventory, and price changes, to slower fab investments, macro-economics and increased geo-political risks. Although many companies have been cautious regarding their spending, innovation continued.

I find in our industry, that no matter what comes our way, we are able to cope and continue to innovate and move ahead. Otherwise, how could a 9.1% compounded annual growth rate (CAGR) be achieved over a four-decade period of time, exceeding the 1 trillion mark in integrated circuit (IC) in 2018 in IC Units?[1] What other industry can show such growth, while bringing to the market such a broad range of technologies and applications with such significant impact on our lives? With this in mind, I was very happy to watch SEMI's new and refreshing video which brings awareness to our industry and the impact it has had and will continue to have on humanity.[2]

Last year, despite the downturn, which forced many companies to implement cost reduction measures and travel restrictions, the events continued to be well attended, showing how important they are for our industry, from learning to information exchange, to marketing, and networking. Companies and academia continue to value and support these activities, even during slower and more difficult times.

Ring in 2020

The industry is recovering from last year's downturn and has started the New Year with expectations for a more positive outlook and growth. As we ring in 2020, there are several industry trends worth tracking that will further drive innovation and growth opportunities across the entire supply chain: more energy efficient products, artificial intelligence (AI), edge computing, further evolution and deployment of connected devices and IoT, even more so as a result of the 5G adoption, quantum computing, etc. All these applications will further drive the increase in semiconductor and electronics content and innovation across the entire supply chain. 2020 will be a year of innovation as the industry continues to better understand how to leverage current technologies for new applications and also to develop new ones.

A Materials Perspective

The next generation of smart devices will continue to drive the need for higher performance, miniaturization, and a greater demand for increased functionality and integration. In terms of packaging, with so many new functionalities being brought into the package or at a system level, the integration of these devices will become increasingly more critical, and this will also apply to the different materials going into the package.

Innovation in materials and integration technologies will continue to play an important role in developing and bringing new devices and systems to production. Looking at the various packaging platforms, fan-out wafer level packaging (FOWLP) will continue to be a hot technology, with several players bringing in their own flavors, either at wafer or panel level. 3D integration using through silicon via (TSV) technology with or without interposers, although introduced to the industry more than a decade ago, continues to find new applications due to its performance benefits, miniaturization and, in some applications, cost savings as well. Supported by wider adoption of copper (Cu) pillar technology, moving to more advanced technology node and increase in higher

Figure 1: Reviewing and selecting the papers to be presented at ECTC 2020 is serious business.

performance computing, will further drive the growth of the flip-chip platform. This platform will continue to maintain its dominance within the advanced packaging sector.

With the growth of mobile and connected devices, IoT, an increased number of sensors, RF devices, and active and passive components are being packaged within smaller and higher performing systems. This trend will continue to be enabled by system-in-package (SiP), which could incorporate many flavors of the above-mentioned packaging technologies. SiP and heterogeneous integration will continue to grow and see increased adoption across various applications, from sensing modules; to logic and memory systems; RF and front-end modules; wireless connectivity; power management; and MEMS modules, to list a few. Advanced packaging, with all of its platforms, has already been in an upward trend, gaining a share in the overall packaging market over the more traditional platforms. By the end of this year, the advanced packaging segment is expected to reach parity, in terms of value, with the traditional packaging segment.

With such a dynamic market, new applications and several packaging technologies available, it will be very interesting to see the evolution and further adoption of these technologies and their future growth.

Important Events and Conferences for 2020

Going back now to events and conferences in 2020, here is a list of conferences I am involved with and looking forward to attend. For those of you who are not that familiar with the packaging space, these are some great events you should not miss this year:

- Heterogeneous Integration Roadmap (HIR) Annual Workshop in February, in Santa Clara, CA. In 2019 we launched the first edition of this roadmap. The annual workshop will give you the opportunity to hear and interact with a large group of industry experts, see the work of all the technical working groups and volunteer in one of these groups. John Hunt from ASE and I are chairing the Wafer Level Packaging technical working group and will gladly welcome new volunteers in our group. More information can be found at https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html
- Device Packaging Conference in March, in Fountain Hills, AZ: the 16th edition of this event, organized by IMAPS, will also include the well-known 3DinCites awards. Don't miss the opportunity to submit your nominations and vote for your favorite technology, company, engineer, start-up, etc. More information can be found at: https://www.3dincites.com/
- IEEE Electronics Packaging Society ECTC Conference in May, in Lake Buena Vista, FL: the 70th edition of ECTC, a

Continued on page 55

In Pursuit of Edge Computing

By Emmanuel Sabonnadière, CEA-Leti

Computing applications are a major driver of the semiconductor industry's advanced technology developments. The sector's continuing evolution over the past 20 years has enabled major innovations and opportunities for investments in two main areas: Infrastructure, where performance and mass storage are essential to address high-performance requirements; and Information processing as close as possible to the data generated, also known as edge computing.

Edge computing applications include cars, distributed computers, and embedded systems like drones and smart watches. It is also important for Internet of Things (IoT) nodes, where it significantly reduces costs and energy consumption.

While complex computation is still performed in a high-performance computing (HPC) infrastructure, edge computing selects and processes critical data locally, close to the data generation, before sending only relevant information to the cloud. The historical, centralized computing world of supercomputers and data centers now coexists with more mobile, autonomous platforms thanks to smart sensors and an increasingly flexible communications infrastructure.

Home assistants today, autonomous vehicles and robots in the near future are good examples of such systems.

Challenges in Edge Computing

The constraints on edge computing, which are quite different from the usual HPC challenges, include:

- Reducing power consumption to guarantee autonomy for the devices and their users
- Specializing functions to handle local processing

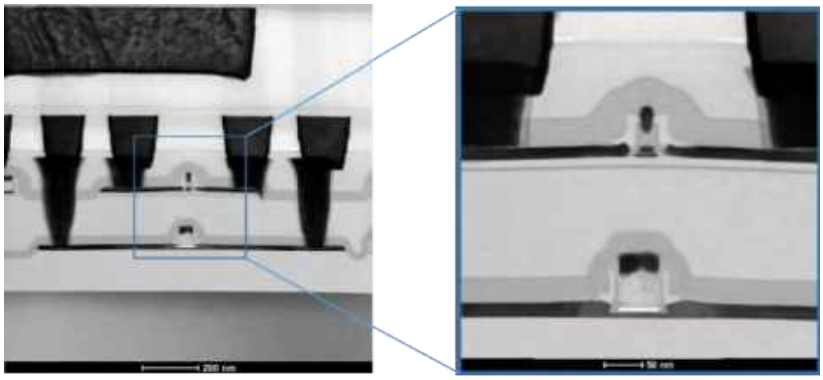


Figure 1: CoolCube™, CEA-Leti's version of 3D sequential integration allows device stacking at nanometer-scale resolutions, allowing for low aspect ratio and small 3D-contact fine-grain interconnects.

- Managing the heterogeneity of multiple functions under demanding cost-and-power limitations: sensing, communication, security, and energy storage

In many applications, low latency will also be important, as in critical decision systems, autonomous driving, or industry of the future. But form-factor limitations in edge computing will also be key to defining the best architectures. Finally, cost and reliability will impose specifications on a case-by-case basis, depending on the final application and environment. Taken together, these various constraints raise a global challenge to find versatile and scalable solutions to the requirements of edge computing.

How are CEA-Leti's 3D Technologies Enabling Edge Computing?

CEA-Leti is focusing on developing technologies that contribute to the convergence of the physical world and processing nodes. This work includes:

- Integration of materials and devices on large silicon wafers that are best tailored for sensing, actuating, communicating, or display functions
- In all cases, this requires co-design activities between the technology, IC design, and system-architecture teams. Indeed, optimal solutions at the edge call for specific solutions to deal with local conditions to full fill the applications requirements.

In addition, clean rooms and their equipment are at the core of CEA-Leti's strategy and model:

- CMOS/FD-SOI for power efficient computing accelerators and evaluation beyond CMOS options such as nanowires and 2D materials
- Substrate engineering
- Advanced embedded memories (PC-RAM, OXRAM…)
- Technologies for imaging and display
- Silicon photonics
- 3D integration technologies with a focus on CoolCube™ and high-density hybrid bonding techniques

Focusing on 3D Technologies for Edge Computing

Interconnect efficiency between functions/dies is key to achieving high performance within a limited power budget. Combined with its embedded memories program, CEA-Leti is working on fine-pitch 3D technologies. From direct hybrid bonding to 3D sequential CoolCube™ integration (Figure 1), the Institute benefits from a broad range of generic expertise required for edge computing programs.

For two examples on how 3D can be used for edge computing's challenges, let's consider a technology dedicated to efficient computing, and then focus on sensing with a smart imager program.

CEA-Leti in the Chiplets Race

To tackle the growing difficulties with CMOS scaling and pursue

technology and design integration in a More-than-Moore manner, CEA-Leti is combining 3D integration, using active silicon interposers and the chiplet concept. This allows further system integration, while reducing the power consumption devoted to system-level communication. CEA-Leti is actively working on the chiplet concept in the frame of the IRT Nanoelec French initiative and has released a proof-of-concept called IntAct (Figures 2a and b).

Figures 2a and b: A 3D multicore circuit called IntAct is said to offer five times more processing power and double the energy efficiency of the best 3D circuits currently available.

Using fine-pitch 3D interconnects increases chip-to-chip bandwidth and limits overall power consumption, while a chiplet approach allows yield optimization with smaller chips and reusable IP blocks.

The IntAct proof-of-concept integrates 96 cores offering a low-power computing fabric with innovative cache-coherent architecture and wide voltage range. The 3D stack is composed of six identical multiprocessor 22mm² chiplets, fabricated in 28nm fully depleted silicon-on-insulator (FD-SOI) technology and stacked face-to-face on a 200mm², 65nm CMOS active interposer by means of ultra-fine pitch Cu pillars. The active interposer integrates innovative features, for efficient system integration, namely — power management to power the chiplets on-demand, system interconnect for providing any chiplet-to-chiplet communication and a system-on-chip infrastructure, including system-level communication IP, clocks, sensors, and test solutions.

Smart Imager Program

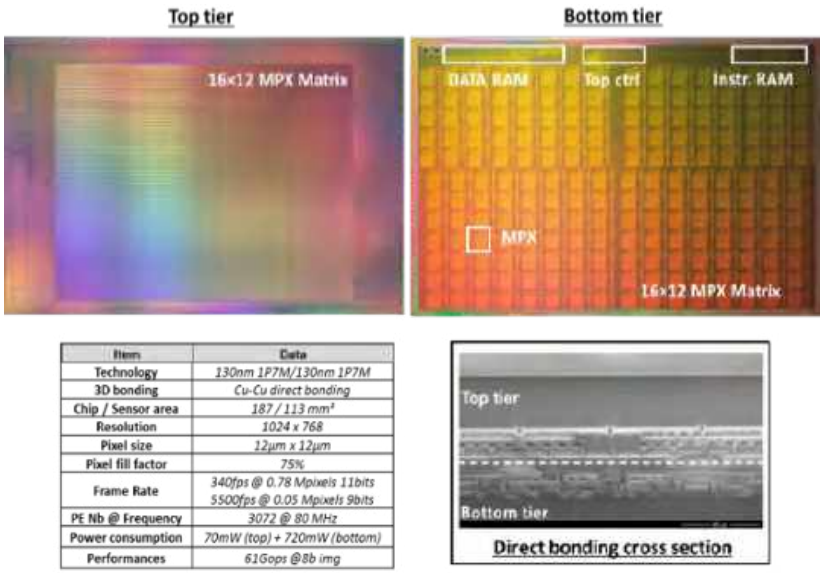
Image sensors will become more and more pervasive. In the context of automotive and, more globally, edge computing, low-cost devices, with high-quality pixels, will embed increasing numbers of smart functions, such as regular low-level image processing, but also object recognition, movement detection, light detection, etc. 3D stacking technology is a key enabler to integrate into a single device the pixel layer and associated acquisition layer, but also the smart-computing features and the required amount of memory to process all the acquired data. More computing and memory within the 3D smart-image sensors will bring new features and reduce the overall system power consumption. Advanced 3D technology with ultra-fine-pitch vertical interconnect density will pave the way towards new architectures for 3D smart image sensors, allowing local vertical communication between pixels, and the associated computing and memory structures. Direct hybrid bonding (with a possible pitch in the range of the µm) and 3D sequential CoolCube™ technology (pitch in the range of 100nm) will provide the interconnect density required for such a system.

CEA-Leti teams have proposed a novel prototype of vision chip called RETINE (Figure 3). It combines a backside illuminated image sensor featuring a fully parallel in-focal-plane readout circuit with a matrix of 3,072 programmable processing elements on the bottom tier, demonstrating a 5,500 fps image sensor with low-latency image analysis. Even the current architecture efficiency can be improved by increasing its embedded memory capacity thanks to a third 3D-layer integration. Some image-processing functions need a global interpretation level that may require extra layers, such as an efficient general-purpose CPU or dedicated accelerators like neuro-engines for direct imaging inference.

Conclusion

In conclusion, CEA-Leti focuses strongly on both HPC and edge computing programs. 3D is considered as a core technology to achieve the best trade-off between performance, consumption, and cost.

NB: This work was partly supported by the French National Program "Programme d'Investissements d'Avenir, IRT Nanoelec" under Grant ANR-10-AIRT-05.



Item	Data
Technology	130nm 1P7M/130nm 1P7M
3D bonding	Cu-Cu direct bonding
Chip / Sensor area	187 / 113 mm²
Resolution	1024 x 768
Pixel size	12µm x 12µm
Pixel fill factor	75%
Frame Rate	340fps @ 0.78 Mpixels 11bits 5500fps @ 0.05 Mpixels 9bits
PE Nb @ Frequency	3072 @ 80 MHz
Power consumption	70mW (top) + 720mW (bottom)
Performances	61Gops @8b img

Figure 3: CEA-Leti's RETINE technology stacks an image sensor and a matrix parallel array of processors in a single vision microchip to provide fast detection and flexible scene analysis capabilities. This reduces the output data stream to the minimal relevant amount.

How the Industry Megatrends are Impacting the Semiconductor Supply Chain

A lot can happen in a year. As 2019 was winding down, we asked you how the industry megatrends like the pursuit of artificial intelligence (AI) and the race to 5G, combined with the uncertain economy and geopolitical situation, are impacting your company. Here's what some of you had to say.

Industry Collaboration Becomes More Critical as Technologies Converge

By Samer Bahou, SEMI

Perhaps more than at any point in history, the semiconductor manufacturing and design supply chain is in the world's spotlight, thanks largely to the recent period of international trade tension. The national agendas of governments representing the world's largest economies are prioritizing IP protection along with chip procurement, the materials involved in fabricating them, and even the talent required for design and manufacturing.

While military technology and national security factor into this sharpened focus on the semiconductor industry at the government level, another key element stems from the increased economic importance of the industry as the broader electronics market supply chain becomes more interconnected with it. There is a universal push across markets and industries to integrate more intelligence and connectivity into applications that have semiconductors as their foundation. The integration of AI, machine learning, and IoT and 5G connectivity is taking advantage of data's status as the new oil. This is creating enormous economic opportunities in the automotive, consumer, manufacturing, and medical markets, and in others as well.

These opportunities have driven some of the world's most powerful companies, including Apple, Google and Facebook, to bring semiconductor design resources in-house to achieve differentiation. However, many more companies are seeking to increase collaboration with their semiconductor supply chain to expedite leaps forward in technology integration. One prime example of this is in the automotive industry, where OEMs are working more closely with semiconductor companies to integrate new electronics and systems on the path to autonomous vehicles. This was evident in 2019 with SEMI announcing that both Audi and Volkswagen joined the industry association as members to strengthen their collaboration with the semiconductor industry.

In this new era of rapidly evolving and converging technologies, there is a critical need for collaboration across the broader semiconductor manufacturing and design supply chain. This is a guiding principle of SEMI's strategy to help the industry and its members thrive. Over the past few years, SEMI expanded its industry allies with five new Strategic Association Partners (SAPs) — Electronic Systems Design Alliance (ESDA), Fab Owners Alliance (FOA), FlexTech, MEMS and Sensors Industry Group (MSIG), and Nano Bio Materials Consortium (NBMC). This amalgamation of technology partners opens the door for broader collaboration.

New initiatives and programs that foster collaboration are also a central component to address the industry's shared challenges and opportunities. SEMI's SMART Initiatives seek to do this for key verticals in the industry, with Smart Mobility serving as one example that has brought together the automotive OEMS mentioned earlier, along with other OEMS and a broad range of suppliers to look at both global and regional issues.

Another example of collaborative initiatives in the semiconductor industry is the Heterogeneous Integration Roadmap (HIR). As we shift from a focus on chip scaling

to system scaling, heterogeneous integration will be at the heart of major innovations right along with intelligence and connectivity. The HIR works to sort through technology issues at an industry level so that investment and R&D can be more focused. Volunteers from around the world, from across the design and system supply chain, and from industry, academia and R&D institutes, meet regularly to set targets for technologies 15- to 25-years out that will ultimately provide guidance for decision-makers. SEMI is one of the sponsors of the HIR effort, helping to provide it with industry validation.

2020 marks the 50th anniversary of SEMI, and the convergence of technologies we are currently witnessing makes it clear that the need for industry collaboration is stronger than ever. Taking part in these efforts allows you to contribute in planning the industry's future, while providing a networking opportunities that can lead to a more successful future for your business.

Optimism Ahead! The Opportunities are There

By Yann Guillou, Trymax Semiconductor

I am writing this viewpoint while 2019 will close in a couple of days. If I try to summarize what happened and what it means for Trymax, here are my key takeaways.

First, I guess many of you agree that 2019 was tougher than expected for the semiconductor industry and this negatively impacted equipment companies. Trade tensions were not positive for the electronics market, and as a consequence, China decided to speed up its domestic IC industry, and Trymax took advantage of this. We have been doing business in China for a long time, but this year we achieved our best sales ever in this region. Prospects for 2020 looks promising, with many new projects expected.

Second, car sales have declined, and the auto IC market was flat due to excess inventory. Nevertheless, for the next few years, significant growth is still expected — IC content in cars will drastically increase with electric vehicles (EVs) and advanced driver assist systems (ADAS). IC semiconductor sales should be up for 2020, and Trymax is well positioned by already being the solution provider for many leading integrated device manufacturers (IDMs) driving this industry, including 300mm wafer size.

Third, wide band gap (WBG) materials such as SiC and GaN seem to be the best choice for energy efficient solutions and the industry is clearly moving in this direction. Many important announcements were made in 2019 by various players in the supply chain — strategic investment, capacity expansion, transition to larger wafer size, etc, At Trymax, while we deal mostly with silicon substrates, we also offer the right products for non-silicon-based materials such as WBG. We look forward to supporting this market in 2020 and beyond.

Fourth, even if its contribution to the global wafer capacity is limited, Europe has significant and ongoing new constructions, expansions, and fabs needing to be equipped. The 2019-2020 period is probably the most dynamic it's been for a long time. Being a European equipment headquartered company, Trymax puts a priority on winning this business. Our first successes came in 2019 and we will do our best to grab more in 2020. Our ambition is clear in this region — we want to remain the market share leader and gain an even higher market share.

To conclude, 2019 had some good moments and second half of the year showed improvements. These are expected to continue in 2020. Some delays might still appear on the journey but the horizon for More than Moore applications is brighter than ever. Let's ride it together.

The Impact of Megatrends

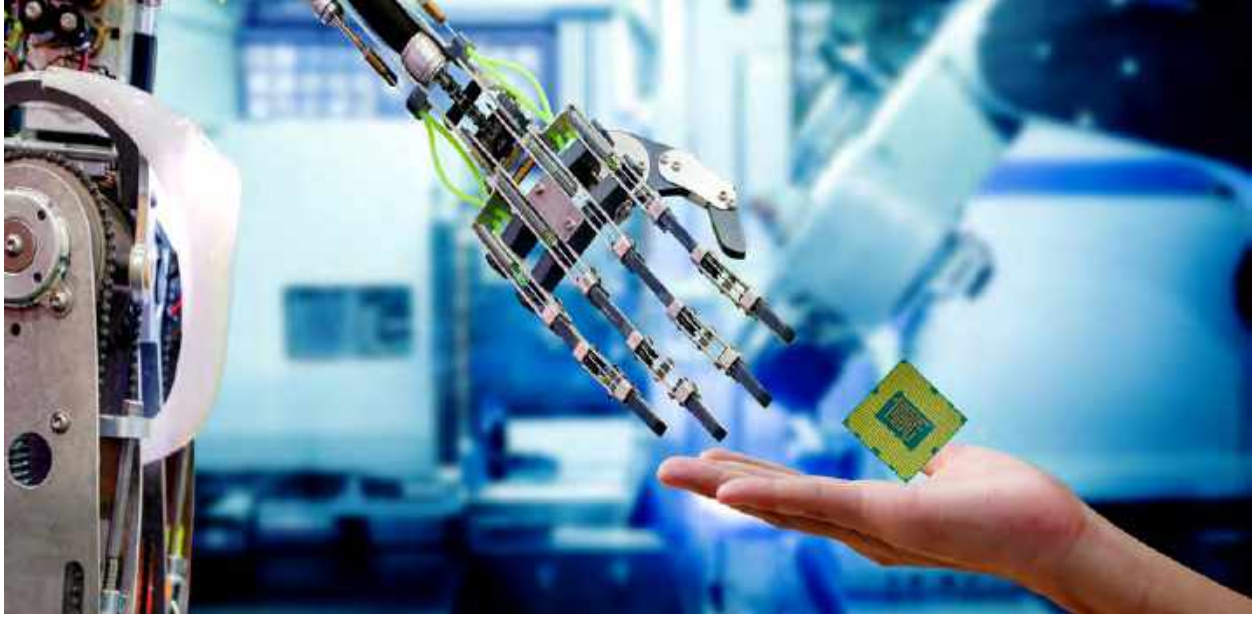
By Keith Felton, Mentor, A Siemens Business

Over the last 2-3 years, everyone has been talking about Moore's "Law" becoming invalid. Even if it does, we will continue to reduce the cost of logic gates, just as we did before solid state electronics was developed. This learning curve is forever — it will continue, but the reliance we have placed upon shrinking feature sizes to reduce costs will not. We will have to innovate in other ways. Satisfying the industry demand for continued increase in electronic functions per unit area is driving packaging innovation. One path is to integrate, on the package, heterogeneous or homogeneous smaller high-yield chips. DARPA is driving number of initiatives around chiplets, functional building blocks that when combined provide the same capabilities as a monolithic system-on-chip (SoC).

But having access to even known-good chiplets still leaves an open question. Primary among them is: What is the best way to combine these chiplets into a working system? Here we meet a double-edged sword. On the one hand, there are lots of established methods: 2.5D integration on a silicon interposer connected through C4 bumps and through silicon vias (TSVs) to the ultimate ball grid arrays (BGAs) that connect to the boards. Then there are simpler connections from die-to-die through super thin, and often very small, bridge-like interposers that do not require TSVs. Then of course there is the well-publicized die-to-die connections through package redistribution layer (RDL) in the form of wafer-level fan-out processes.

Going to full 3D opens up even more options. Two or more components may be stacked with a combination of direct bonding and TSVs. Using through-mold-vias (TMVs), opens more methods to integrate across stacks. While some of these approaches — such as chip-on-wafer-on-substrate (CoWoS) style using silicon interposers or fan-out wafer level packaging (FOWLP) using package RDL — continue to gain in popularity, it is clear that none of these approaches are likely to go away.

Ultimately the choice of how to best integrate chiplets will depend on the design requirements. While this seems daunting, it ultimately



allows more ways for engineers to differentiate their final offerings. Of course, one of the big challenges this creates is how to determine which approach ultimately will be best. This is not trivial. The best approach is to digitally prototype the complete package assembly so early predictive analysis can be used to evaluate approach viability. This drove Mentor to develop its high-density advanced packaging (HDAP) solution, in which a true 3D virtual model of the package assembly can be constructed and then analyzed not only for routability, signal, and power integrity but also for structural performance such as thermal stability and thermally induced stress.

We learned that a design solution for this new breed of packaging must be able to cope with a level of design capacity never seen before; yet deliver real-time performance and be available on Windows as well as Linux. To achieve this, we began applying foundry proven technology to an emerging process that is more foundry-like than it is traditional organic laminate package-like. Of course, foundries capture their IC processes as process design kits (PDKs) in order for their customers to efficiently design and obtain high-yield results. So, in conjunction with OSATs such as Amkor, the package assembly design kit (PADK) was created to support and drive the adoption of these new packaging technologies and help fabless semiconductor and systems companies to easily transition. HDAP is the new platform for "More than Moore" to achieve electronic functions per unit area scaling, and Mentor is a committed leading-solution supplier with its Xpedition and Calibre technologies.

Successful Growth in 2020 Calls for a Strategic Approach

By David Wang, ACM Research

On the whole, 2019 was a very interesting year for the global semiconductor industry. After a record 2018, the market saw a decline caused by a softening memory market, coupled with an uncertain geopolitical climate. The U.S.-China trade war, in particular, has impacted semiconductor equipment suppliers based in the United States.

On the positive side, China continued to invest in a self-supporting semiconductor ecosystem, while technology megatrends like artificial intelligence, machine learning and 5G drove developments in both front-end and advanced packaging technologies. This helped create business opportunities for materials and equipment suppliers.

There is also an industrywide push to be more environmentally aware. Many manufacturers are taking steps to reduce the amount of sulfuric acid (H2SO4) waste produced during wafer clean processes.

At ACM Research, in our quest to become a leading global provider of semiconductor equipment to both foundries and outsourced semiconductor assembly and test service providers (OSATS), we have factored in all of the above conditions to plan our growth strategy for 2020.

Since we opened our Shanghai Operational Center in 2006, our tools have been on the lines of top-tier semiconductor and memory manufacturers, as well as OSAT providers throughout China, Korea, and the Philippines. In 2017, we completed our NASDAQ IPO in the U.S., and in 2019 we ramped our U.S. team and capabilities. Our pending IPO in China will help solidify ACM's position as a key local player in China, while helping to fund the continuing development of our world-class capabilities.

We believe being listed in two stock markets will allow us to scale our business in mainland China, and also open up broader opportunities in the U.S., Taiwan, Korea, Japan, and Europe. A key element of our growth strategy is to be close to customers, world-class engineering talent, our supply chain, and to our investors.

In 2020, we will continue scaling our efforts in the U.S. by offering differentiated, leading-edge technology, along with localized service to our fast-growing customer base, supporting advanced nodes, 3D memory and wafer-level packaging.

Diversity, Parity, Prosperity: Perspective of an Industry Veteran

By Paul Werbaneth, Consultant

It's been more than forty years since I earned my degree in chemical engineering from Cornell University, and my professional career in the semiconductor device manufacturing and packaging industries now spans five decades, starting with me as a newbie process engineer in an early Intel 4" wafer fab, and continuing, to this day, writing this piece for you.

And my perspective on Japan — having lived and worked there starting in 1984, and with a family member, my daughter, currently on an expat assignment as an operations manager for Netflix in Tokyo — has been informed by almost as many years as my semiconductor industry tenure.

Gender diversity, parity, and inclusion in professional organizations (and in academia), or lack thereof, has been much studied. McKinsey&Company, for example, issued an update to their *Delivering Through Diversity*[1] report in January 2018; McKinsey's conclusions about Inclusion and Diversity (I&D) are these:

The relationship between diversity and business performance persists

The statistically significant correlation between a more diverse leadership team and financial outperformance demonstrated three years ago continues to hold true on an updated, enlarged, and global data set.

Leadership roles matter

Companies in the top-quartile for gender diversity on executive teams were 21% more likely to outperform on profitability and 27% more likely to have superior value creation.

It's not just gender

Companies in the top-quartile for ethnic/cultural diversity on executive teams were 33% more likely to have industry-leading profitability. That this relationship continues to be strong suggests that inclusion of highly diverse individuals — and the myriad ways in which diversity exists beyond gender (e.g., LGBTQ+, age/generation, international experience) — can be a key differentiator among companies.

Figure 1: SEMI WiS Panel 2019, L-R: Bika Carter, GlobalFoundries; Christina Chu, Energetiq; Mukta Farooq, IBM Research; Amy Leong, FormFactor; Sophia Rogalskyj, CSNE

There is a penalty for opting out

The penalty for bottom-quartile performance on diversity persists. Overall, companies in the bottom quartile for both gender and ethnic/cultural diversity were 29% less likely to achieve above-average profitability than were all other companies in our data set. In short, not only were they not leading, they were lagging.

The McKinsey study on the business impact of inclusion and diversity presents clear and compelling conclusions favoring increased diversity as a must-achieve top objective for any business striving for competitive advantage.

Yet I&D progress, overall, has been slow.

I can't really address the question about why I&D 'inertia', if you will, exists, although the obvious answer suggests itself.

Rather, in this perspective of mine for 2020, let's consider what we as an industry are actively doing about inclusion and diversity, doing it because we're smart, doing it because we think improving our industry I&D quotient will improve competitive advantage at the enterprise level, and doing it because, frankly speaking, it's absolutely the right thing to do.

Consider SemiSisters. Kudos to Françoise von Trapp, for looking toward the future from the year 2013 in the post: "SemiSisters: Factoring in the X."

"Regardless of our profession — whether we are engineers, scientists, technologists, market analysts, or executives; or came to the industry as marketing, journalism, and PR professionals — what ties us together is the understanding that there's something significant about being a woman immersed in the male-dominated semiconductor industry."[2]

From those 2013 beginnings, 3D InCites/SemiSisters has profiled

Figure 2: Françoise von Trapp presents the first SemiSister Award to Cornell University's representative, Jeff Berg.

and promoted the work of an outstanding array of female scientist and engineers, including Dr. Mary Jane Irwin, Department of Computer Science and Engineering at Pennsylvania State University; Dr. Lena Nicolaides, KLA; Rozalia Beica; Dr. Maaike M. Visser, Disruptive Technologies AS; Jessica Gomez, Rogue Valley Microdevices; and, in this issue of The Yearbook, Severine Cheramy, CEA-Leti.

Excellent role models all.

Consider the SEMI Women in Semiconductors program, now one of the highlights of the SEMI Advanced Manufacturing Conference week (Figure 1). As Amy Leong, FormFactor, reported from WiS 2019 via 3D InCites, "Now in its 4th year, more than 140 attendees were at this event, up from about 60 attendees four years ago. Titled 'Building Your Network — Crucial Connections,' the WiS panel explored the vital role networking plays in the success of women throughout various stages of their careers, as they pursue opportunities and overcome challenges."[3]

Christina Chu, Energetiq, adds about SEMI WiS 2019 "Companies that recognize their top performing female employees as leaders provide examples to the whole world of how women lead in their industries. Employees see what a female leader 'looks like' and women at the company have role models."4

And do companies provide recognition solely based on altruistic motivations? Maybe, but then there's also the call of competitive advantage, because "having more women in the labor force easily translates to increased profits."

Congratulations to Margaret Kindling and her colleagues at SEMI for the I&D spotlight at WiS/ASMC, at the various SEMICONs of the world, and for both talking the talk and for actually walking the walk — even in Japan.

Consider E. Jan Vardaman, TechSearch International, and the committed effort she and her colleagues have made establishing the IEEE Frances B. Hugle Engineering Scholarship, which honors the memory of Frances B. Hugle and her many significant engineering accomplishments. Frances co-founded Hugle Industries, Siliconix, Stewart Warner Microcircuits, Inc., and Opto-Electronics Devices, Inc.; in each of these companies she served as a director of R&D and as chief engineer. She held 16 known patents in the field of electronics, and was one of the pioneers in the invention of tape automated bonding (TAB).

May the scholarship provide the resources for many more female engineers to follow in Frances' footsteps, including the 2019 award recipient, Caitlyn Patton.

And consider please the Cornell University College of Engineering.

Why?

Well, when I think back to my first week of freshman year at Cornell Engineering I remember the famous session, seated in a large lecture hall, where we were asked to turn right and look, turn left and look, and then to consider that by the time graduation rolled around one of those two people, Mr. Right, or Mr. Left (they were almost exclusively misters), would be gone. (Of course, it wouldn't be you gone … or would it?)

What about Cornell Engineering today? I'm sure it's still a challenging program, and the incoming students are so much more accomplished than I was going in, but, in terms of diversity and parity

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SPOTLIGHT:

SemiSister Success Story: A Woman on the Edge of 3D Technology

By Françoise von Trapp

Severine Cheramy,
3D Business Development and ITR 3D director at CEA-Leti

Severine Cheramy has devoted her career to developing 3D integration technologies and bringing them to market. We first met when I visited CEA-Leti's cleanroom in 2009 during my Tour de France in 3D. At the time, she was a project leader working under Nicolas Sillon, lab manager. Little did I know that we would become SemiSisters, and that 10 years later, she would be leading 3D business development at CEA-Leti as the IRT 3D Director.

When she launched the 3D VLSI Workshop a few years ago, 3D InCites partnered with her and CEA-Leti to promote it. About a year ago, we sat down to talk about her journey, and I thought this issue of The Yearbook was the perfect opportunity to tell her story.

Farm to Fab

Cheramy grew up on a farm in Normandy. Her family raised goats. She was the youngest of three, with two older brothers. She says it wasn't so natural growing up on a farm to go study science, but she always loved physics, chemistry, and math. "My parents let me do what I wanted, provided I worked hard at school," she says. "They always encouraged me."

Cheramy earned a general engineering diploma in Engineering, with a focus on physics and math. She didn't set out to pursue a career in the semiconductor industry. Her first job out of university was in the aeronautics industry. After a year, she moved on to Schlumberger, an international oilfield services company. That was in 2000, when the company was investing in emerging technologies like sensors used in oil exploration and smart cards used in banking. Schlumberger spun off its smart card division, Axalto (now merged with Gemplus as Gemalto). There she worked on component development for product lines like SIM cards, biometric passports, and contactless payment systems.

In 2008, she joined CEA-Leti as project manager in 3D, and the rest, as they say, is history. She went on to become lab manager, business development manager, and then director of IRT 3D. Her work has focused on developing bonding processes for 3D ICs.

Overall, Cheramy is happy with her chosen path in the semiconductor industry. "I'm proud of my evolution," says Cheramy. "I'm always learning — thanks to my colleagues and my work environment. I haven't changed between many companies in 20 years." Even when I asked about low points in her career, she couldn't come up with one.

She finds working in R&D and industrial research for the semiconductor industry exciting because she is always learning, and there is constant change. As director of business development, it's her job to identify what could be the next trend in 3D in the next 3-5 years. "As CEA-Leti is not publicly funded, we need to anticipate the next industry's trends and convince the industry to invest in technology and in CEA-Leti," She explained. "We also make sure our engineers are anticipating the future. I follow the news to see what is needed to enable the next technology trends."

Does she ever wish she had chosen a different path? Cheramy says in her teens, she had a passion for theater, and would have pursued an acting career if her parents had agreed. But they saw it as a fun pastime, not a job. Now that her own children have become "fully autonomous" she has gone back to acting for fun. She says it helped her in her work by making her more comfortable speaking in public. In this industry, where so few women present at conferences, it's a great skill to have.

What Success Looks Like

The greatest challenges Cheramy faced in her career occurred during her studies, when she was only one of two women out of 40 in all classes (physics and math) except for chemistry. But those numbers are changing. In fact, there is a strong initiative in France to promote science and engineering in high school, and the numbers of women are increasing. No longer will you find only two or three women in a class of 40.

Cheramy's advice to young women who want to pursue a career in the semiconductor industry: "Don't be

Figure 1: at ECTC 2019, with Severine Cheramy (right) and her CEA-Leti colleague, Coralie Gallis (left).

scared. In France and in the world, the students with the best high school grades are women. The reason they don't continue excellence in performance is fear. They think they need to do better."

Additionally, it is possible in France to combine a professional and family life. "When you have children, you can stop working for few months, and still come back at the similar level that you were at before," she said. "You can also work part time and be a soccer mom." Cheramy said that both in the public and private sector, this work-life balance is supported by employers and the government.

Cheramy measures her success by the fact that every day, she comes to work and leaves happy. While not everyone can say even that, I think she is being humble. She participated with the global 3D teams to achieve 1µm pitches in wafer-to-wafer and to reach die-to-wafer approach with direct hybrid bonding. CEA-Leti is also launching a multi project wafer as part of Leti's CoolCube™ program, a true VLSI 3D IC solution. If that doesn't describe a woman on the edge of 3D, I don't know what does.

Diversity, Parity, Prosperity: Perspective of an Industry Veteran continued from 42

(or equity), it's been a sea change in Ithaca.

Per Cornell, "With the arrival of the Class of 2022, the Cornell University College of Engineering now enrolls equal numbers of undergraduate women and men — the first engineering school of its size and stature to achieve this milestone. Particular gains have been made in computer science, where female students once comprised a fraction of the department. Achieving gender equity at the College of Engineering was decades in the making, a product of advocacy at the university's highest levels."

Achieving gender equity at the Cornell College of Engineering was literally decades in the making.

Imagine the effort.

Applaud the result. I do.

Others as well: And the inaugural SemiSister Award goes to … Cornell University College of Engineering (Figure 2).

Announcing the award in March 2019, Françoise von Trapp wrote: "New this year, as part of our SemiSister Project, we established the 3D InCites SemiSister Award, to recognize organizations, companies or individuals who are doing the most to foster gender diversity and inclusion in the semiconductor workplace. To me, this may be the most important recognition this year, as industry-wide awareness grows around this issue. The four nominees included Cornell University College of Engineering, FRT- The art of metrology, Brewer Science, SPTS Technologies, and Leslie Tugman, representing SEMI. … This year's winner by 3280 votes is Cornell University College of Engineering for reaching parity in women to men in its engineering program with the enrollment of the class of 2022. These students are our future."

These students are our future. Which is why my perspective 2020 is an optimistic one.

Sure, there's still too much inertia holding I&D back, but we-in-the-know know that continuing to improve our industry's I&D quotient will improve competitive advantage at the enterprise level, and who doesn't like that.

Besides, we know it's absolutely the right thing to do on the human level. And who doesn't support that.

Diversity, Parity, Prosperity in 2020 and beyond — will you rally with me?

From Pittsburgh, PA, thanks for reading.

1. *"Delivering through Diversity," McKinsey&Company, January 2018, retrieved from https://tinyurl.com/y86q92s8*

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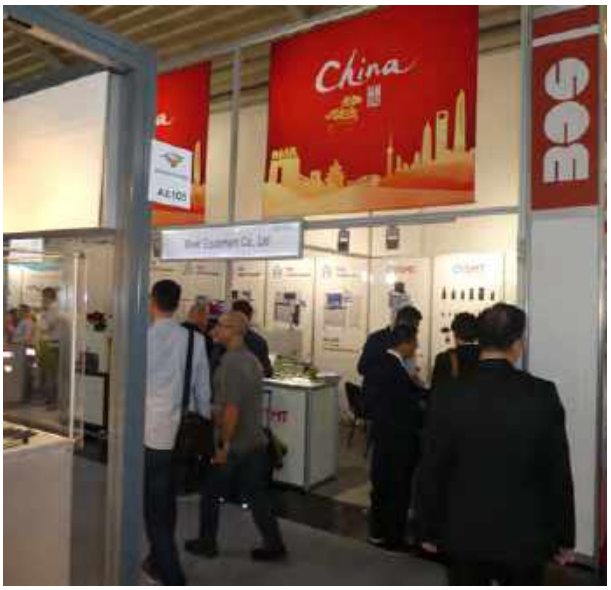

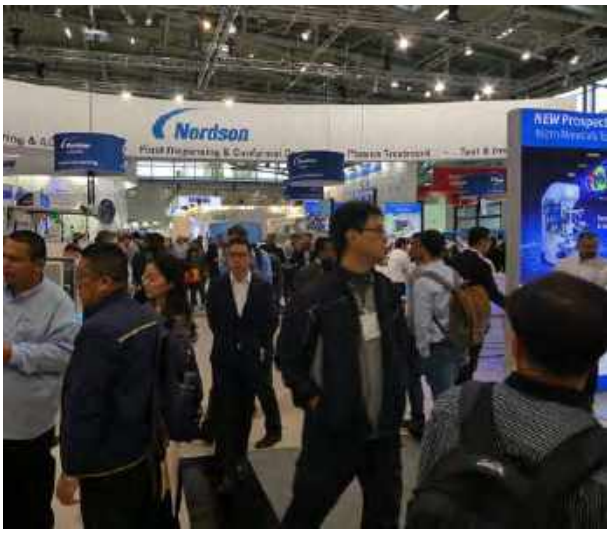

SEMI Sisters

MOMENTS

The Evolution of Advanced Packaging continued from 17

inspection and metrology was minimal. The rise in process complexity for advanced packaging schemes is changing this traditional way of thinking. Inline defect inspection is an established means to quickly identify yield limiters and improve learning cycles in the front end of semiconductor manufacturing. The advanced development in packaging is causing back-end manufacturers to follow a similar trajectory, requiring more inline inspection steps with much higher sensitivity, leading to rapid process advancements to continuously improve yield. A fast learning cycle has big implications for profits, and with the increasing number of diverse packaging technologies being adopted in advanced packaging manufacturing, inline inspection can help provide the data required for process control at the source. After all, you can't fix what you can't find, and you can't find what you don't look for.

Heterogenous integration adds complexity and presents a two-fold challenge. The first is making sure that the overall package meets performance specifications. This involves verifying the yield of each individual component, and subsequently, ensuring the yield and the power performance of the combined system with all its connections meets the integration objectives.

The second challenge is that heterogeneous integration is highly application-specific so there is no common interconnect scheme that guarantees the best performance for all given architectures. Inline inspection and metrology will be key to accelerating learning cycles to advance the development required to optimize interconnect architecture. With an HDFO architecture, line and space dimensions continue to shrink towards 1µm or potentially even smaller, and these features sizes require process control to stop yield excursions from even smaller defects. Hybrid bonding technology, in wafer-to-wafer and die-to-wafer variations, is another exciting architecture that can provide enhanced capability by reducing interconnect pitches down to a few microns. The complexity in this process comes with its own set of challenges where process control will be critical. Cu pad profiles need to be tightly controlled with a precisely engineered recess, overlay specifications need to be very tight, and the bonding surfaces need to be free of even submicron defects, which could cause voids.

The Right Solutions

The type of process control required for the successful development of new advanced packaging architectures has evolved along with the technology. Smaller feature sizes, new integration schemes, and the heterogeneous integration of multiple components into single packages all bring tighter process control requirements. Not only is there a need for greater sensitivity to find smaller defects of interest, but there is a need for additional inspection steps to ensure traceability and process control at the source. The high cost of end-of-line yield excursions provides additional incentive for foundries, IDMs and OSATs to expand their process control solutions to keep pace with the current packaging roadmap. These new process control requirements demand enhanced inspection and metrology. This measurement capability is only possible in systems that feature custom hardware, such as innovative illumination sources, optics, and sensors. With the Kronos™ CIRCL™-AP and ICOS™ product lines, as well as targeted application of its front-end portfolio, KLA brings decades of technological leadership in process control along with a track record of innovation, to continue to solve challenging packaging problems and enable tomorrow's most impactful technologies.

Why AI needs 3D Heterogenous Integration continued from 15

chiplets, as well as vertical power and communication. Ramune Nagisetty, Senior Principal Engineer, Intel, stated at IEDM, that 3D packaging technologies such as EMIB and Foveros would enable system engineers to choose what they think are the best of breed chips for their specific application and create a SiP. This capability could be a key driver in making AI more affordable and energy friendly.

At Hot Chips, Intel introduced its Lakefield core, leveraging Foveros 3D stacking technology to manufacture a set of chips for mobile edge applications. Competitors are hot on Intel's heels, either leveraging TSMC's CoWoS technology, or developing similar packaging technologies that will enable AI deep learning to take place.

At ARM TECHCON 2019, ARM presented on the multicore technologies that the company believes will be needed for deep learning. I would expect rapid development of the heterogenous packaging technologies as the demand for edge compute grows (Figure 3).

The size of the market for edge computing or mobile-edge computing is somewhat nebulous and it will depend upon where these heterogenous packages are placed. Gartner has the IoT endpoint market reaching 5.8 billion in 2020 increasing about a billion units over 2019. It is unlikely most endpoint applications will need AI at the edge, but if 20% of those do there is a billion-unit market. However, it is more likely heterogenous packaged systems will end up in gateways or small server farms that are near the endpoints, so a more likely number for high-end heterogenous packaged systems would be in the hundreds of millions, which is still a significant market.

Heterogenous packing will be one of the key components in the growth of the AI market place. The ability to create a SiP using best of breed chips will help to reduce the cycle time of the learning process, as well as potentially help to reduce the amount of energy needed to develop the models that are needed to help proliferate AI in everyday business.

2019-2020: A Year of Contrasts Vs. A Year of Innovation & Growth continued from 35

premier packaging conference of the industry, with mroe than 1700 attendees, 380 technical papers in 36 technical sessions, 5 Interactive presentation sessions, 18 professional development courses and several panels, special sessions, receptions, and networking opportunities. As the program chair of this event, I am working with several industry colleagues (more than 200 volunteers) to organize what I anticipate will be a great event. I am very excited about the 2020 program. We will address various important topics and industry trends, from photonics, to quantum computing, AI hardware, all the different packaging platforms, heterogeneous integration, and various applications. The Plenary Session this year will focus on 3DIC: Past, Present, and Future and will have, as all the other special sessions and panels, a distinct list of industry experts. This is one event you cannot miss! More information at: https://ectc.net/

- Strategic Materials Conference, a SEMI event, in September, in San Jose, CA. I have the honor to chair the conference this year together with Lin Tso from Semi and Katherine Hutchinson from Versum, and work with a great group of leaders from various companies across the supply chain. The planning has already started and, we will bring to this conference, keynote talks, economic and geo-political discussions, emerging technologies, including packaging, metrology, and a start-up and VC focused session. Find more information at https://www.semi.org/en/connect/events/strategic-materials-conference-smc

With that, I would like to take this opportunity to thank all the volunteers involved with these conferences and roadmap activities. All others interested in volunteering participating, please do not hesitate to reach out to me.

On a personal matter, 2019 was a good year. I am very thankful to all the challenging, nurturing, and inspiring experiences I had in 2019 and looking forward to an even better 2020.

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Chiplets: The New Era Begins continued from 13

an active interposer removes the bottleneck of memory proximity. Intel is expected to leverage the technology across many product lines.

Conclusions

Chiplets are a heterogeneous integration solution that can move us into the next semiconductor era. While it is technologically possible to continue scaling monolithic die, the economics do not favor this approach. The use of chiplets will become a game changer in the new era for companies that can master the design of this new approach.

New players are emerging that will help others participate in the bold new chiplet era. California start-up zGlue offers an online tool, called ChipBuilder, to build chiplets to connect to its smart silicon interposer that allows the use of third-party chiplets. The chiplets, fabricated as wafer level packages (WLPs), can be connected to an active silicon interposer called Smart Fabric. The company has created a library of more than 250 off-the-shelf chiplets and plans to extend it to more than 1,500 in the near future. In this new era, fortune favors the bold that are able to apply smart packaging as a solution.

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How AiP Technology Helps Enable 5G and More continued from 26

- A smaller footprint-phased antenna array design to minimize space
- Reduced signal attenuation for mmWave products
- Lower power consumption
- Improved range for devices
- A design proven and qualified by the supplier

In fact, Amkor's AiP/AoP packaging technologies have achieved over 60 GHz operation.

Design Services & Design/Production Capabilities for AiP/AoP

For AiP/AoP technologies, Amkor has developed an extensive toolset to maximize circuit density and address the sophisticated packaging formats required for high-volume production of 5G and any mmWave design. In addition to an advanced multi-die integration toolbox and RF SiP design and simulation know-how, other capabilities include:

- Extensive fcCSP, WLCSP, LDFO and HDFO portfolios for multi-die designs
- An established and reliable supply chain
- Global assembly scale and system test investments
- RD design & measurement lab

Initiating an AiP/AoP Design

Amkor offers many options to incorporate AiP/AoP in a variety of packages or SiP and the high-volume production capacity to support the design of the next generation mmWave products. To integrate Amkor's market leading 5G and mmWave packaging technology in a next generation application, system designers simply need to contact Amkor and discuss their system requirements.

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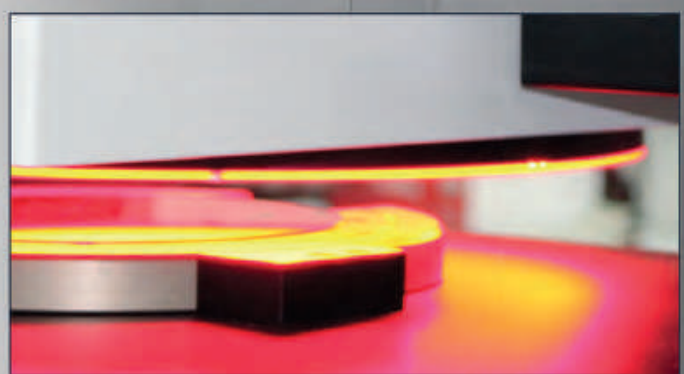
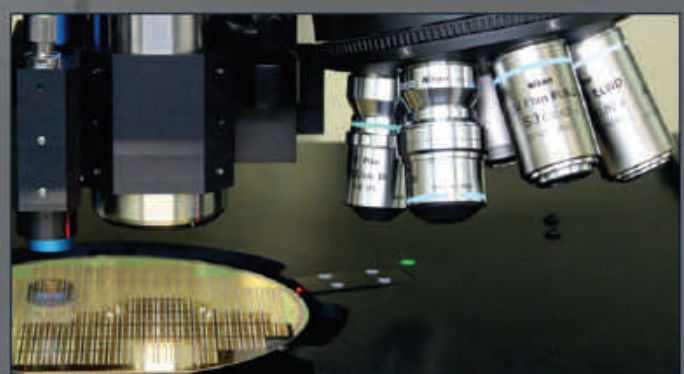


Defect inspection setup with singleshot, step module and microscope station



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