3DInCites™ EST. 2009

YEARBOOK

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The 3D InCites Yearbook is published by:
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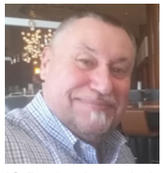

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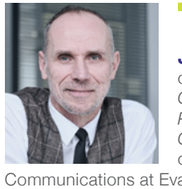

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Looking Back on 2020 and Moving Forward into 2021

COVID-19 hit the world in early 2020 with very little warning. The semiconductor industry was poised for recovery, and all market indicators pointed to solid growth. For many of us, reality hit with the announcement that SEMICON Korea was cancelled the day before it was set to start. Soon after, SEMICON China was postponed, and an industry dependent on global travel to conduct business was left hanging. What ensued was a very different kind of year than the one we anticipated.

If there is one thing we learned from 2020, it is how important it is to have a contingency plan. For event organizers, that meant pivoting quickly to shift from physical events to virtual ones. For equipment and materials suppliers, it meant learning how to conduct business without spending 80% of the time visiting customers around the world. For semiconductor manufacturers, it meant bolstering the supply chain to keep up with increasing demand because the world was working, learning, and socializing from home.

In January, Herb Reiter represented 3D InCites at the SEMI Industry Strategy Symposium in Half Moon Bay, CA, and Steffen Kröhnert wore our colors at the 3D System Summit in Dresden. IMAPS decided to still hold the Device Packaging Conference in Fountain Hills, AZ, from March 2-5, 2020 by adhering to a strict no-handshake policy while doling out bottles of hand sanitizer. This meant we could host the 2020 3D InCites Awards Ceremony in person. Check out the photos beginning on page 56.

Once events turned virtual, we covered more news and events than we ever had, simply because the information was merely a laptop click away. We had our own virtual booths, we Zoomed our interviews and I sat through many presentations. Our entire blogging

team — including Phil Garrou, Herb Reiter, Dean Freeman, and me — divided and conquered. Sadly, however, after 7 years of serving as our 3D InCites EDA evangelist for 3D integration, Herb Reiter retired at the end of October. Those shoes will be difficult to fill, but we're going to try.

While we all missed the hallway chatter and the in-person networking of physical events, we discovered new ways to connect. Relationships grew deeper and more personal, as we Zoomed into each other's homes, and met pets, kids, and partners. Business casual was replaced by hoodies and t-shirts as we literally let our hair down.

At 3D InCites, we were lucky. Ironically, 2020 was the year we hit our stride. We launched our new community-centric platform, essentially providing our growing membership with a virtual venue that is always available. Trine Pierik, who joined the team in 2019, took on the daunting role of Community Director, keeping our virtual booths and member activities humming along, and supporting me behind the scenes with day-to-day tasks. Together, we helped FRT, ERS Electronic GmbH, and SEMI celebrate milestone anniversaries. And in this issue's cover story (Page 22), we tell the story of the people behind DBI.

By the end of the year, 45 companies joined the community and were active participants. For example, Kiterocket and ERS Electronic GmbH had local teams attending SEMICON China, the only physical event that took place, and each provided interesting blog posts and the photos that appear on page 60. Beginning on page 50, check out how our members navigated the pandemic, and what their predictions are for 2021.

For me personally, the silver lining of COVID-19 was growing the SemiSister network. What started out as local happy hours with SemiSisters in the Phoenix metro area has grown into two monthly social events: Happy Hour for the Pacific time zone, and a global social hour attended by SemiSisters worldwide, whether it's for breakfast, lunch, afternoon coffee, or a nightcap.

And we've got big plans for 2021.

As the semiconductor industry strives to improve sustainability practices, we're dedicating a new blog topic to it, authored by Dean Freeman and other guest experts. Additionally, to expand our commitment to diversity, equity and inclusion, we're establishing an endowment fund to support technology businesses that are owned by women or under-represented minorities. The fund will be seeded by proceeds from the 3D InCites Awards program, as well as other efforts. I can't wait to see what else this year brings. All of us at 3D InCites wish you continued success!

Francoise

Figure 1: ERS Greater China Sales and Marketing Director Joshua Zhou presenting at this year's CSPT

Doing Business in China: A European Company's Perspective

By Sophia Oldeide and Chengxu Huang, ERS Electronik

China consumes more than 50% of all semiconductors annually. However, with a rapidly growing consumer market, domestic Chinese manufacturers can meet only around 30% of their own demand.[1] A statistical report from China Electronic Production Equipment Industry Association (CEPEA) shows that the domestic market self-sufficiency rate of integrated circuit equipment is only about 5%, and the self-efficiency rate of the IC front-end equipment market is even lower.[2]

Despite the technical gaps in some semiconductor production processes, China has significantly increased its competitiveness in assembly, testing, and packaging of electronics over the past two decades, making it an attractive market for equipment suppliers. However, navigating and establishing your business in a foreign market means adapting to and adopting certain practices. Here are some things we have learned about the Chinese business world since we opened our sales office in Shanghai in 2018.

Getting to Know the Industry

Advanced packaging is one of the fastest-growing semiconductor market segments in China. Thus, many advanced packaging-related events take place there every year, including the SiP Conference, SYNAPS, and the all-encompassing SEMICON China. While many event organizers had to move their events online this year, those in China were able to open up for in-person events again in the summer, adhering, of course, to strict hygiene and safety regulations.

Thanks to our team on-site, we were not only able to attend these events but also to present at the China Semiconductor Packaging and Test Market Technology Annual Conference (CSPT), one of the most prominent advanced packaging conferences in China (Figure 1). The conference has been exclusive to Chinese companies in previous years, but this year, possibly due to COVID-19, they allowed non-Chinese companies to attend. Exhibiting and presenting at regional events like these is crucial in order to be seen by the local big names in the industry and to learn about the latest market developments. CSPT, for example, presents an industry forecast for the upcoming year, which many domestic companies use to outline their annual plan.

Email or WeChat?

As in any industry in any part of the world, communication is a vital component for a well-functioning business relationship. In Germany, email is the primary business communication tool, and especially this year many of us started using Microsoft Teams, Zoom, or Skype to hold meetings. If a company intends to raise its brand awareness or build-up a business network, it may choose LinkedIn as a corporate social media platform. In China, however, instead of using various applications in parallel, WeChat, which integrates all the functions mentioned above, is the go-to app for people's work and private life. As its creator Tencent announced earlier this year, there are 1.151 billion WeChat active users per month.[3] Especially in big cities, such as Beijing, Shanghai, and Guangzhou, WeChat has become the default digital platform for social interaction, also with business partners. For example, instead of exchanging business cards, the Chinese will often invite you to scan their WeChat QR code (Figure 2). And although it may seem invasive, do not be afraid to use WeChat to ask business-related questions. You will not only get an answer, but you can also expect to receive it a lot quicker than via email.

In 2019, there were over 1 billion WeChat users overseas, and although privacy is still a concern among western users, the use of WeChat seems inevitable to those who want to expand their business in China.

Figure 3: Our ERS Greater China team at SEMICON China 2020

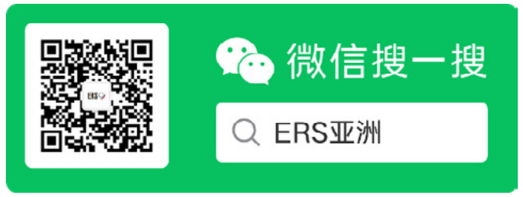

Figure 2: This year we started a company WeChat account, where we regularly post company news and industry updates

Bridging the gap between cultures

Learning the language, culture, and customs will always be beneficial if you want to enter a foreign market. China is often characterized by a high-context culture, which suggests that context and non-verbal cues tend to be more meaningful to the conversation than the actual spoken words. On the other hand, Germans are known for their directness and honesty in conversations, which can be interpreted as arrogance or impoliteness by the Chinese. Having native Chinese members in your team is, therefore, not surprisingly, a considerable advantage (Figure 3).

Not only is it essential to have a team of locals — you also need a local support team. A seven-hour time difference and adherence to different calendars (Lunar vs. Gregorian) can make it difficult to build solid business relationships.

Joshua Zhou, Sales and Marketing Director of ERS Greater China, says that offering local support is a huge selling point. "This is a fast-paced industry, and companies don't have time to wait several weeks for technical support and service. Shipping defective products back to Germany for repair is both time-consuming and expensive. This year has shown that we cannot always rely on easy and fast travel overseas and has really highlighted the importance of building a local support team."

While this may seem obvious, we find that it's still worth mentioning, as it's important to remember that customers, regardless of where in the world they are located, are quite similar.

"The Chinese market is often mystified by other countries. However, in our experience, it is not much different from any other market in terms of customer needs and wants. They want reliable and quick service and support, preferably in their native language, which is hardly unique to China," says Laurent Giai-Miniet, CEO and CSMO of ERS.

It's been almost three years since we opened our office in Shanghai, and we are still learning new things, which is to be expected in such a rapidly evolving industry and market. Thanks to our team, not only in China, but also worldwide, our focus can remain on providing the best possible solutions and services to our customers. After a tumultuous year, we are excited to see what awaits us in 2021!

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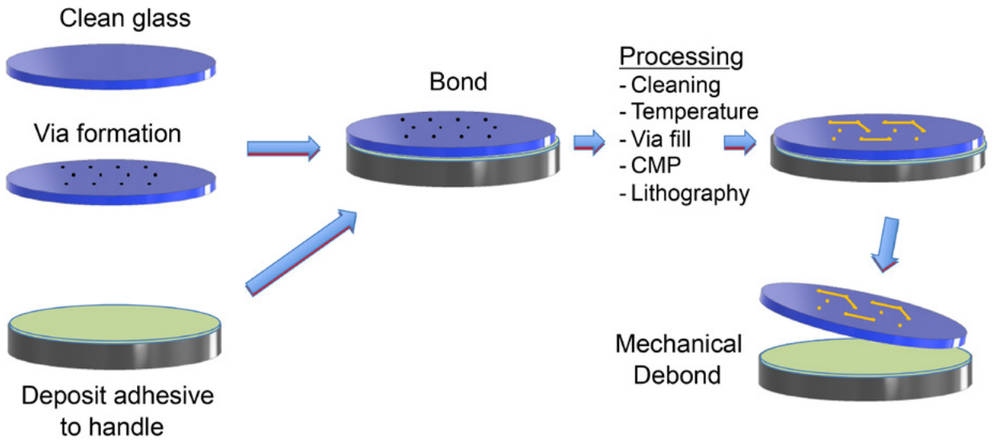

Figure 1. Overview of Mosaic thin glass handling solution

Solutions for Glass-based Packaging are Here

By Aric Shorey, Mosaic Microsystems

A number of research articles have been published over the past several years showing the advantages glass-based solutions can bring to packaging and systems integration including radio frequency (RF) front-end devices, interposers, MEMs devices, and integrated photonics. In particular, RF applications for glass are gaining interest for use as a substrate for filters, switches, and mm-Wave antenna arrays. The advantages include low insertion loss, as the frequency increases above a few GHz, relative to Si-based solutions; and higher integration density and much lower roughness compared to laminates and ceramics. Furthermore, we have seen numerous articles from universities, glass companies, and important members of the semiconductor supply chain (including TSMC, ASE, GlobalFoundries, and others) showing successful demonstration of glass-based devices with impressive quality metrics, such as very low insertion loss compared with Si, demonstrated reliable performance and high Q-factors.

The question, is, with all of this interest and activity, why has glass not become more of a mainstream product? In fact, we heard from end-users at conferences in 2020 that through glass via (TGV) technology is still not ready. The biggest challenge, of course, has been maturing the supply chain to enable smooth transition from small-scale demonstration to high volume manufacturing (HVM).

Mosaic Microsystems is changing this narrative with their handling solution that utilizes the Viaffirm™ bond and Si handle wafers. The approach uses a thin inorganic adhesion layer to temporarily bond a thin glass wafer (with or without TGV) to a silicon or glass handle wafer (Si handle wafer is the primary approach) (Figure 1). The thin glass substrate is then processed through downstream steps such as via fill, chemical mechanical planarization (CMP), redistribution layers (RDL) passive deposition, lithography and bumping. The key is that the bond is stable (remains temporary and does not outgas) to more than 400 °C. Utilizing a Si handle wafer allows the thin glass products to be fabricated leveraging existing equipment and processes, with only a mechanical de-bond that can be accomplished using existing solutions.

A key aspect of this handling solution is that it addresses the gaps in the supply chain that have hindered the adoption of glass-based solutions. It is important that this solution integrate seamlessly into typical back-end processes, which includes via fill, CMP, RDL, de-bond and dicing/singulation without significant changes or upgrades required of existing process equipment.

To achieve integration, the strength of the bond is optimized to sufficiently enable downstream processing, but then be able to be de-bonded mechanically with low force. Depending on customer flow, this could take the form of transferring directly to dicing tape for die size dicing/singulation, transferring to another handle wafer for backside metallization, or permanently bonding to another wafer for further wafer-level packaging. Since the bond strength can be adjusted, this approach can also be used to create multi-wafer structures while also integrating passive devices, antenna and/or switches as appropriate, making it

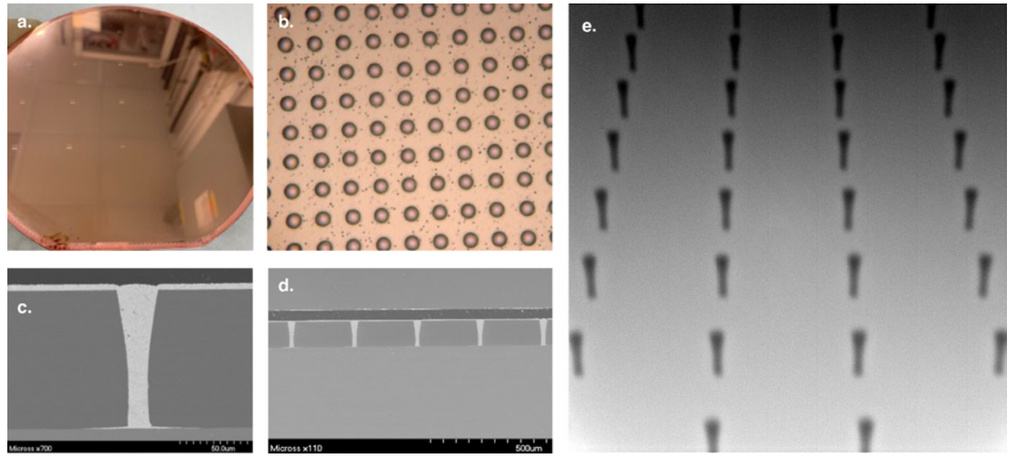

Figure 2. Copper plated glass-on-silicon wafer. a) whole wafer as plated. b) top view of dense area of vias. c) individual via, showing footer and void-free fill. d) Lower magnification SEM view of a dense array of vias. (a-d courtesy of Micross) e) X-ray tomography of a section of plated wafer (Courtesy of AIM TAP, Anthony Lisi)

attractive for incorporating glass in many potential products.

A key aspect of this process is that when the thin glass with TGV is temporarily bonded to the handle wafer, the vias look like blind vias similar to through silicon vias (TSV). This allows you to plate the vias much like you would a TSV, which at this point is a mature process, while avoiding the need for back-grinding and polish steps. This makes glass via fill readily available to the supply chain and is a step change in the manufacturability of glass substrates. A good example of this is summarized in Figure 2. Wafer stacks with Corning Incorporated's SG3 glass at 100µm thickness and TGV with 30µm top diameter were provided to Micross AIT for via metallization. The adhesion layer consisted of 100nm of Ti, followed by 300nm of Cu. Using its advanced plating chemistry, Micross was able to fully fill the vias in 100µm-thick glass, with only about 4µm of overburden on the surface.

Figure 2a is a photograph of the wafer after plating, while Figure 2b shows the top view of the plated vias. The SEM cross section image of a single via in Figure 2c shows the complete fill of the via. Figures 2d and 2e show the consistency of the fill, and no voids by cross-section and X-ray respectively.

To achieve a via with good planarity, overburden often needs to be removed by CMP. Several bonded wafers were sent to Axus Technologies in Phoenix, AZ, for CMP. The wafer stacks were handled with the same conditions as for standard silicon wafers, and all polish runs completed successfully with no damage to the glass. Figure 3 shows an image of a metallized wafer post-CMP. All of these demonstrations were completed in the first lot of wafers, underscoring how well this approach ties into existing processes. Similar demonstrations have been done for plating/patterning (Figure 4), de-bond and multi-wafer stacking demonstrating suitability to leverage existing solutions to fabricate devices on glass <200 um thick.

Summary

The material properties of glass make it an attractive material for next-generation applications, particularly in RF and heterogeneous integration applications. For this reason, there has been a great deal of interest over the past decade to leverage glass solutions, but challenges to implement these solutions in a high-volume environment has slowed adoption. This new temporary bonding technology provides a path for high volume implementation of thin glass solutions and represents a significant increase in the readiness for fabrication of glass-based devices.

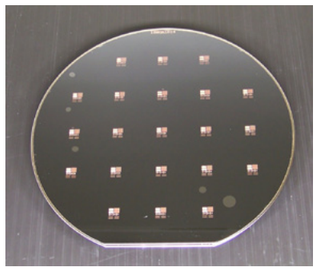

Figure 3 Thin (100µm) glass on Si handle after via fill and CMP

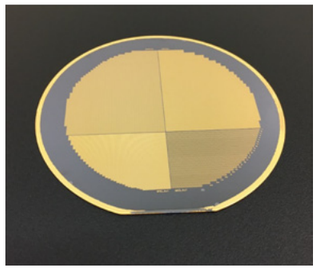

Figure 4 Thin (100µm) glass after Ni/Au plating and patterning

Fine-Pitch 3D Stacking Technologies for High-performance Heterogeneous Integration and Chiplet-based Architectures

By Peter Ramm, Fraunhofer EMFT; Mustafa Badaroglu; Qualcomm; Paul Franzon, NSCU; Phil Garrou, MCNC; and Pascal Vivet, CEA

3DIC Integration in its true definition has a long history.[1] Richard P. Feynman expressed this vision in 1985: “Another direction of improvement of computing power is to make physical machines three dimensional.”[2] Successively, several research and development (R&D) initiatives started world-wide. in the late 1980s, in a German consortium comprising Siemens, Philips, and Fraunhofer Munich, 3D CMOS test devices as 3D SRAMs were realized based on recrystallization of thin Si.[3] Such monolithic concepts are reconsidered today as “the ultimate 3D” for stacking at transistor level — in the International Roadmap for Devices and Systems (IRDS) for the 2030s.

Early 3D IC Developments

Towards the end of the 1990s Mitsumasa Koyanagi´s team at Tohoku University succeeded in fabricating 3D ICs using through silicon vias (TSVs) to create 3D stacked image sensor and 3D stacked memory test chips.[4]

This represented the pioneering contributions of today´s two key applications in high volume production.

Simultaneously, Fraunhofer in Munich was focused on the key application of heterogeneous systems, consisting of components with different materials/technologies and die sizes. Robust die-to-wafer stacking technologies were developed to achieve what is now called 3D heterogeneous integration.[3,5]

But despite these early demonstrations, it wasn’t until 2015 that Samsung produced a high volume 3DIC product; stacked DDR4 and later second-generation high bandwidth memory (HBM2) memory. CMOS image sensors also went into high-volume production.

In 2017, Sony ramped production of stacked CMOS image sensor (CIS) for smart phone cameras. Even so, there were setbacks. Most significantly, 3D memory-on-logic applications, widely forecasted by many sources, have been postponed several times.

Why 3D Integration?

Essential driving forces for 3D integration are performance (speed), power consumption, costs, and form factor. While TSV technologies using advanced intermetallic compound (IMC) bonding or hybrid bonding processes provide very high vertical interconnect densities, the major issue is the high manufacturing cost. Nevertheless, TSV technology shows up as packaging mainstream for high performance 3DICs. However, alternative concepts “between 2D and 3D” were very successful for products with no need of such high interconnect performances, i.e. Si interposer technology. And moreover, alternative interposer concepts avoiding costly TSV technology are gaining importance, as e.g. Intel´s omni-directional interconnect. Figure 1 shows all of these stacking technologies available today.

The Heterogeneous Integration Roadmap has defined corresponding architectures between 2D and 3D. As examples, TSMC´s CoWoS and Intel´s EMIB[6] are categorized as 2DS architectures, Inactive Si, with TSV and without TSV, respectively.

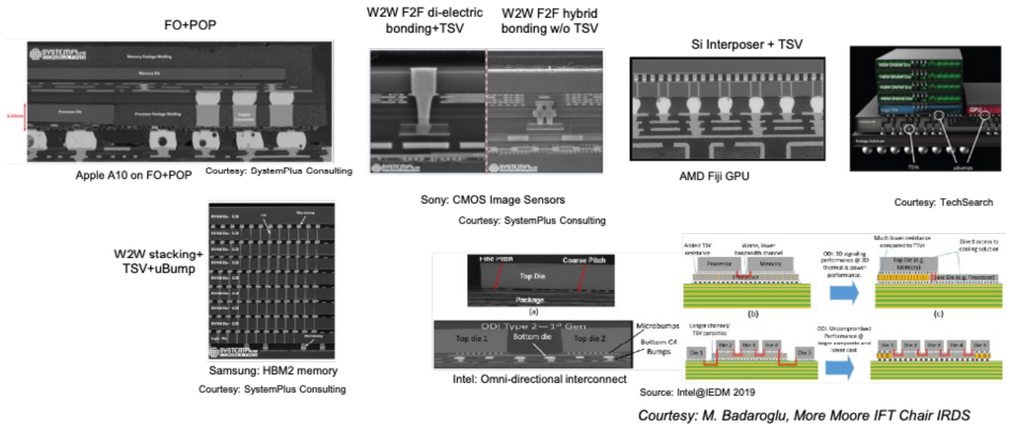

Figure 1: Fine-pitch 3D stacking technologies today

Dis-Integration is Underway

We have known for some time that with lateral scaling slowing down, the industry would need to find another way to continue moving forward. One of the options being implemented is to actually “disintegrate” SoCs into their functional parts and then connect these “chiplets” back together on high density interposers.

Building complete circuits from pre-verified chiplets is gaining traction as a way of cutting costs and reducing time to market for heterogeneous designs. Chiplets allow us to use the latest node only where needed, which in turn results in reduced silicon cost. These silicon savings, in turn, can be allocated for more expensive packaging solutions.

AMD, Intel, and TSMC have all introduced or announced chiplet-based products and/or technologies. It is also widely accepted that mixing and matching chiplets produced at different foundries will require standard interfaces and communication protocols. This is currently the most important thing we can do to stabilize and broaden the chiplet infrastructure. The hope is that these functional chiplets will create a library and in the future, we can combine these tested chiplets from multiple foundries to devise future circuits.

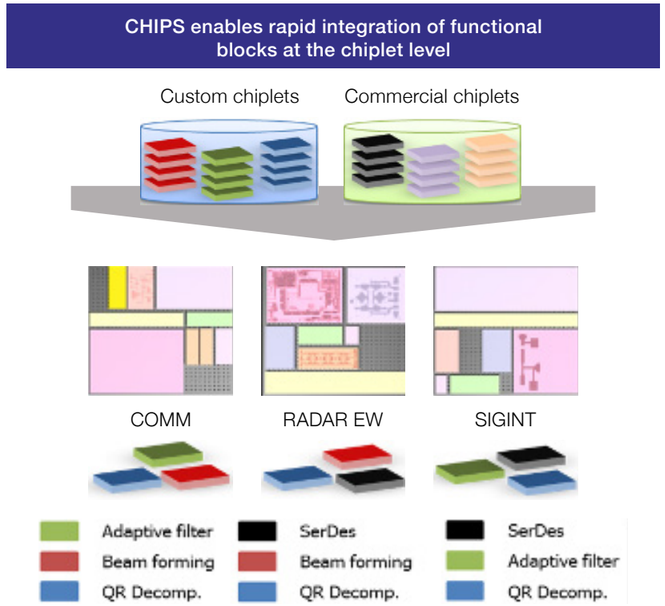

Figure 2: DARPA´s CHIP concept

The US Department of Defense (DOD) Defense Advanced Research Projects Agency is in year four of its Common Heterogeneous Integration and IP Reuse Strategies (CHIPS) program, which has been looking at chiplet based solutions for the military (Figure 2).

Chiplet Physical Interfaces

A key enabling technology is the chiplet-to-chiplet interface. There are several layers to such an interface including protocol and physical layers. The ideal physical layer interface would achieve the power and area footprint of a long range on-chip SOC driver/receiver pair while enabling a high aggregate bandwidth, being able to drive a wide range of wire lengths (with the attendant range of line losses) and support standardized design-for-test (DFT). Key decisions include voltage swing, serialization, clock management, bus-widths, etc.

A number of chiplet interfaces have been proposed. These proposals and some salient features are summarized in Table 1.

Standard	Source	Bandwidth Density/edge	Throughput / lane	Delay	PHY energy/ bit
Advanced Interface Bus (AIB)	Intel[7]	504 Gbps/mm	Up to 2 Gbps	<5ns	0.85 pJ/bit
Multi-Die IO (MDIO)	Intel	1600 Gbps/mm	Up to 5.4 Gbps		0.5 pJ
High Bandwidth Memory (HBM3)	JEDEC[8]		4.8 Gbps		0.37 pJ
XSR/USR	Rambus/OIF		112 Gbps		
Lipincon	TSMC[9]	536 Gbps/mm	2.8 Gbps	<14 ns	0.486 pJ
Bunch of Wires (BOW)	OCP/ODSA[10]	1280 Gbps/mm	Up to 16 Gbps	<5ns	0.7 pJ
Bandwidth Engine	Mosys[11]		Up to 10.3 Gbps	<2.4 ns	
Infinity Fabric	AMD[12]		10.6 Gbps	<9 ns	2 pJ

Table 1: Summary of chiplet interfaces

Chiplet Integration onto Active Interposers

Large-scale interposers for chiplet integration have been fabricated using various technologies, such as 2.5D passive interposers, organic substrates, and silicon bridges. These technologies are mature with economic benefits, but still raise limitations. Due to wire-only interconnects, inter-chiplet communication is still limited to side-by-side communication reducing the number of connected chiplets; the

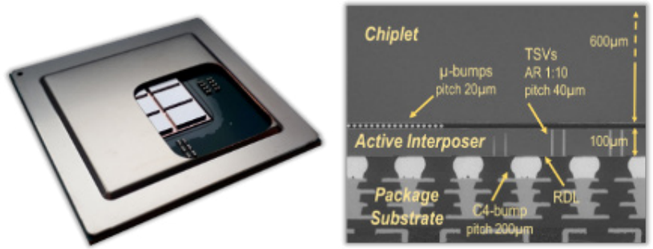

Figure 3: IntAct active interposer and 3D cross-section

passive interposers cannot carry any functions; and finally, co-integration of chiplets with incompatible interfaces is impossible.

To tackle these issues, the concept of active interposer is introduced by integrating some active CMOS circuitry on a large-scale interposer. The active interposer can be seen as a generic bottom die infrastructure which integrates i) flexible and distributed interconnect fabrics for scalable chiplet traffic, ii) energy efficient 3D-plugs using fine pitch interconnects, iii) power management feature for power supply closer to the cores, and iv) memory-IO controller and PHY for off-chip communication. Finally, the active interposer integrates 3D DFT to enable known-good-die (KGD) strategy. Being of low computing complexity and reduced power budget, the active interposer does not exacerbate the thermal issues of the 3D device.

As an active interposer prototype,[13] the IntAct circuit is composed of six identical chiplets (28nm FDSOI) each integrating 16 cores, 3D stacked with fine-pitch (20µm) micro-bumps on an active interposer (65nm CMOS) using TSV middle (Figure 3). The active interposer integrates distributed interconnects for low latency long distance communication, 3D-plug achieving 3 Tbit/s/mm^2 bandwidth density, and fully integrated switched capacitor voltage regulators. The circuit implements a total of 96 cores with a scalable cache coherent architecture, delivering a peak 220 GOPS. Thanks to this partitioning and 3D fine pitch, users get more GOPS at the same power budget and benefit from an increased memory-computing ratio along the memory hierarchy.

As mentioned in the above section, 3D communication standards are strongly required to enable true chiplet compatibility, active interposer is however a solution enabling to bridge incompatible chiplets by integrating ad-hoc bridge logic.

For energy efficient computing, chiplet-based partitioning and 3D technology is driven by two main trends:[14] heterogeneity (as presented in reference [15]) and pitch reduction for energy efficient interconnects for increased coupling between memory and computing. 3D pitch reduction will continue thanks to hybrid bonding technology applied to chiplet integration, with reduced pitches (10µm and targeting below).[16]

Architectures between 2D and 3D — best-tailored for the different specific applications of heterogeneous integration.

Architectures between 2D and 3D are best tailored for the different specific heterogeneous applications. The different applications, e.g. memory, CMOS image sensor, GPU, radio frequency ICs (RFICs), and chiplet-based products, need best-tailored technology solutions for their specific performance, power consumption, costs, and form factor requirements.

Besides 3DIC integration in its strong definition, a variety of architectures between 2D and 3D are potentially well-suited for cost-effective production. This is especially true for the growing market of heterogeneous 3D sensor/IC systems with the need for robust die-to-wafer stacking of components of significant different device technologies, as CMOS, sensors, actuators, and MEMS[17,18] rather than extremely small TSV/pad pitches.

A corresponding example of a heterogeneous 3D sensor integration is shown in Figure 4. The photon detector and appropriate read-out IC are 3D integrated

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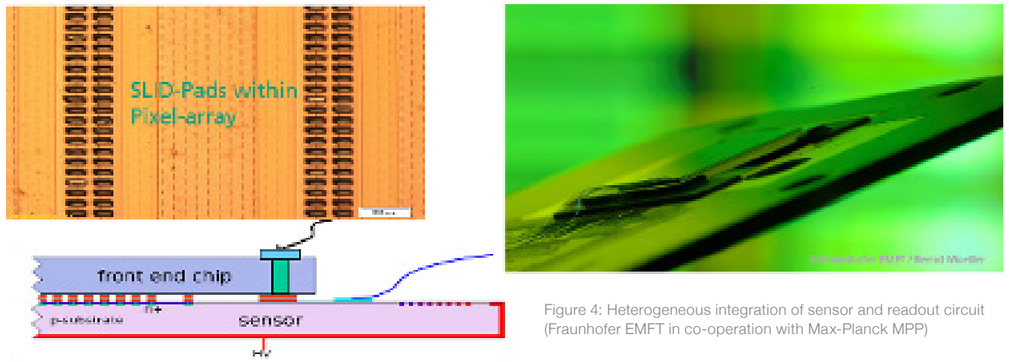


Figure 4: Heterogeneous integration of sensor and readout circuit (Fraunhofer EMFT in co-operation with Max-Planck MPP)

The Future is Heterogeneous Integration

By William Chen, Ph.D., ASE Group

2020 proved to us that our world is wholly unpredictable. As the year began with optimism for a new decade and excitement for what the new decade might bring, the last thing expected was the arrival of COVID-19. Within a short time, the pandemic created unprecedented disruption while shattering lives across the globe. Everything changed, and nations, industries, businesses, and people sought to quickly mobilize and establish best practices to navigate through the challenging days and months that have ensued. A huge debt of gratitude is owed to healthcare and essential workers that have faced risk head-on and sacrificed so much, and who continue to do so while the COVID-19 threat continues to surge.

Accelerating the Digital Transformation

The last year also demonstrated the extent to which technology is being used to solve some of the world's greatest challenges. With digital transformation already on the horizon, the global pandemic meant that our world leapfrogged years ahead and the timeline for work from home, distance learning, and telemedicine significantly sped up. The future became our current reality, as technology was used across the globe to maintain continuity and mitigate disruption.

According to the Consumer Technology Association, there are 14.2B connected things in use and that number is expected to grow to 55B by 2025. This is resulting in an explosion of data. Our connected lives generate 2.5 quintillion bytes of data daily, driving unprecedented demand for bleeding-edge digital networks, connectivity, storage, memory, edge to cloud computing, and so much more. Data has become the oil fueling innovation growth across society, from health to entertainment, from home to business.

2021 has seen the role of the semiconductor industry further thrown into the spotlight. Since the industry began, applications from mainframe to minicomputer to PCs to the mobile space have inspired innovation and growth. It is well known that Moore's Law has driven the industry for decades, but in recent years, there has been a deceleration in terms of performance and economic benefit. The exponential cost of silicon scaling has created an inflection point for the industry, and that is driving the development of More-Than-Moore technologies to augment increased device and system performance.

A Brief History of Semiconductor Roadmaps

Heterogeneous Integration refers to the integration of separately manufactured components into a higher-level assembly system-in-package (SiP) that in the aggregate provides enhanced functionality and improved operational characteristics. It is now the key technology direction going forward, driving the pace of advancement for greater intelligence and connectivity, higher bandwidth and performance, and lower latency and power per function, all at a more manageable cost.

The semiconductor industry comprises highly specialized yet closely interdependent companies that must stay on top of technology and market application trends to keep developments on track. It has been that way since the industry began in the 1950s, but as it grew, it became imperative by the 1990s that measures had to be taken to ensure that global semiconductor companies were progressing in the same direction. Industry leaders bandied together and reached a consensus to work side by side to establish a technology roadmap.

In 1991, semiconductor companies in the United States, under the auspices of the Semiconductor Industry Association (SIA), first established the National Technology Roadmap for Semiconductors or NTRS. By 1998, roadmapping efforts had expanded when companies from Japan, Europe, Korea, and Taiwan joined the NTRS effort, and together with SIA, they formed the International Technology Roadmap for Semiconductors or ITRS. SIA brought ITRS to a close in 2015, and that is when the Heterogeneous Integration Roadmap, or HIR, was initiated.

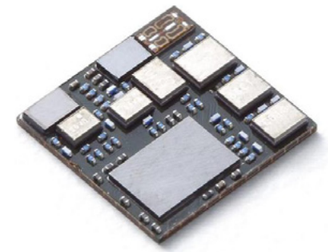
Heterogeneous Integration Will Take Us Forward

Just as Moore's law led the advancement of the global semiconductor industry over the past 55 years, heterogeneous integration is and will be the key technology direction going forward. It is positioned to initiate a new era of technological and scientific advances to continue and complement scaling into the future. Packaging – from device packaging to system packaging – will form the crucial vanguard to this enormous advance.

The Heterogeneous Integration Roadmap (HIR) is a roadmap to the future of electronics that identifies technology requirements and potential solutions. The primary objective is to stimulate pre-competitive collaboration among industry, academia, and government to accelerate progress. HIR is designed to provide long term continuity and a broad technology base. It is organized with sponsorship by three IEEE Technical Societies (Electronics Packaging Society, Electron Devices Society, and Photonics Society) together with SEMI and ASME Electronics and Photonics Packaging Division (EPPD). Technology takes a long time to develop and mature, and increasingly involves the collective knowledge from overlapping fields. It is therefore essential to set goals for the long-run and cover as many subjects and fields as possible, related to heterogeneous integration.

Towards that end, the HIR is organized into 22 technical working groups (TWGs) covering diverse fields in the electronics industry comprising numerous experts and scientists from different disciplines across the globe. Recognizing that technology advances will be driven by advances in system integration in response to market applications, the HIR identifies six market application areas that will shape the electronics industry. These include high-performance computing and data centers, mobile applications, Internet of Things, automotive electronics, aerospace and defense, medical healthcare, and wearables. TWGs are grouped into these six market applications, as well as five building blocks technologies, eight cross-cutting technologies, and three integration technologies. Overall, the HIR contains 23 chapters including the executive summary.

As the industry enters the digital transformation and exascale computing era, massive compute with frequent access to data is required for high-performance computing (HPC) applications. The increasing amount of data from all sectors is raising the issue of operational and storing cost of the data. The advent of artificial



intelligence (AI) and machine learning (ML) requires large amounts of data to be processed and is driving an entirely new computing paradigm from edge computing to cloud to data centers.

Traditional IC design trends call for packing more transistors on a monolithic die or system-on-chip (SoC) at each process node, resulting in difficult chip scaling for the integration of analog, logic, and memory circuits. The heterogeneous integration approach is die-partitioning or chiplets, which offers a compelling value proposition for yield improvement, IP reuse, performance, and cost optimization, as well as time-to-market reduction.

Chiplet integration has the potential to allow the integration of disparate technologies from multiple suppliers to provide more flexible mix-and-match systems to accelerate performance and improve power efficiency without requiring the deployment of these technologies across an entire SoC simultaneously. Chiplet solutions start with internal designs within a system integrator. However, as IP interface standards are developed, the commercialization of chiplets in the market will proliferate. Heterogeneous Integration through chiplets will play a critical role for future HPC and AI/ML applications.

As a leading semiconductor packaging, test, and system service provider, ASE has heavily invested in both chip-level (SoC) package integration and system-level integration. The development of cutting-edge heterogeneous integration technologies addresses functional areas from silicon integration, power integration, optical integration to system integration that form the backbone

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Novel Approaches to Wafer Handling

By Chip Maschal, Eshylon Scientific

Economics are forcing semiconductor manufacturers away from traditional 3D through silicon via (TSV) packaging integration. The future of advanced packaging continues to evolve towards chiplets and innovative new ways to combine specialized microelectronics components. This allows manufacturers to streamline the production for individual "subassemblies" that can then be configured later into functional products.

Emerging system-in-package (SiP) designs include not only memory and logic modules, but also MEMS sensors, radio frequency (RF) transceivers, and optoelectronic components. The race to improve chip density is pushing the envelope of flip-chip packaging, requiring double-side processing of the device assembly. Individual chips might come from 300mm silicon wafers, from 100mm gallium arsenide (GaAs) slices, or anything in between.

Due to the varying sizes and interface diversity of the substrates, device handling becomes an issue. Assembling such disparate elements into a single package typically requires temporarily bonding devices to a carrier wafer and performing a number of bonding and debonding steps to process them further down the production line. An intact wafer might be attached to a carrier for backside processing, or for bonding face-to-face with another wafer. Singulated dice might use a temporary carrier for gang-bonding to an interposer.

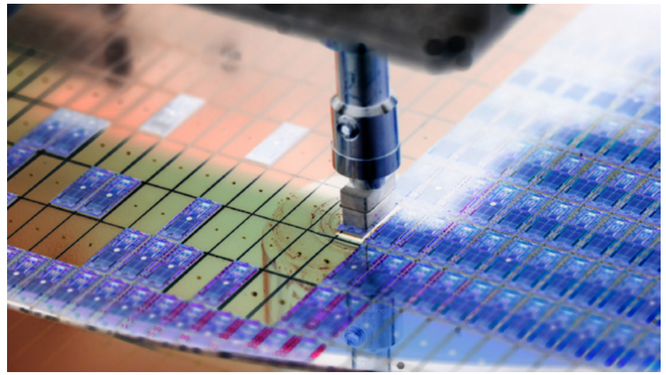

Figure 1: Wafer-level packaging requires a temporary carrier system to support the delicate wafer during the die placement process.

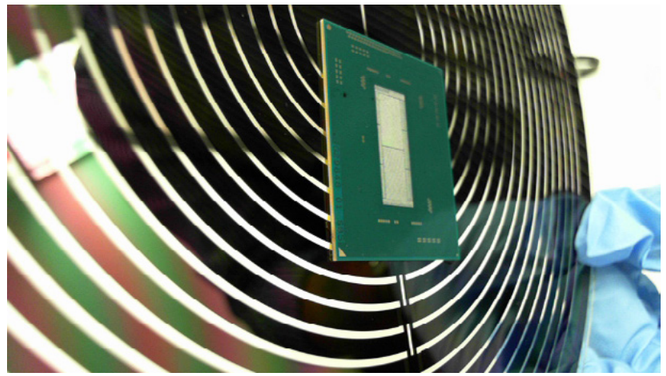

Figure 2: A mobile electrostatic carrier (MESC) system eliminates the need for adhesives.

Temporary Bonding With Adhesives

Typical bonding approaches include adhesives, waxes, and tapes. Regardless of the application, though, each temporary bond generally requires at least five processing steps:

- Clean the wafer surface
- Coat the wafer, the carrier, or both with an appropriate adhesive
- Align the wafer to the carrier, form the bond, and cure the adhesive

Then, once the temporary bond has served its purpose:

- Use heat, a laser, or mechanical force to separate the two surfaces
- Clean the wafer surface to remove any adhesive residue

Each step poses a damage risk. In all cases, residue and contaminants must be cleaned off of the packaged parts, risking yield loss. Thinned dice and GaAs wafers, in particular, are quite difficult to handle. Bonding and debonding requires specialized equipment and unique process chemistries. Also, mismatch in the coefficient of thermal expansion (CTE) between the carrier wafer and the device die can induce wafer warpage or even device damage during some high-temperature cure processes. Often, the bonding adhesive is less thermally stable than the wafer, limiting the available process window.

Electrostatic Carriers: An Adhesive-free Approach

Eshylon Scientific's mobile electrostatic carrier (MESC) system uses no adhesives or tapes,

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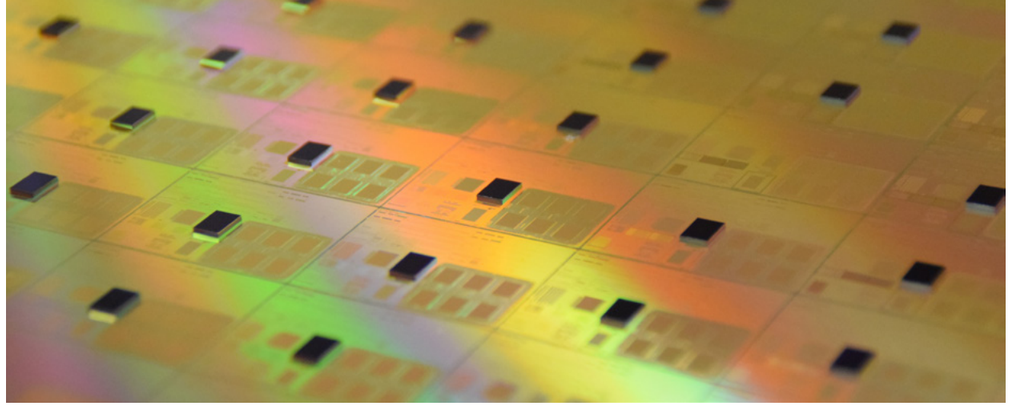

Figure 1: Die-to-wafer: make connection with 3D technology

3D: The El Dorado of Heterogeneous Integration

By Severine Cheramy, CEA-Leti

From the cloud to edge computing, the quest for ever greater power efficiency remains researchers' top priority. From high-end niche to mass-market applications, the best cost-to-performance tradeoff is key to providing a competitive advantage. While Moore's Law has helped meet the performance required in terms of data transfer and power efficiency so far, including for high-end applications such as high performance computing (HPC), it is no longer relevant when it comes to cost-sensitive applications such as edge artificial intelligence and internet of things (IoT) devices.

This presents researchers with difficult choices: can they afford to pursue advanced node performance? Must they find a trade-off, with a risk of inhibiting product performance? And can heterogeneous integration be the solution that will enable decades of future innovation?

CEA-Leti researchers may not have a final answer yet, but their recent results in this technique, including die stacking and monolithic 3D integration, suggest a potential way through the cost/performance dilemma.

Heterogeneous strategies: From greater density...

Vertical 3D integration technology enables stacking chips in a device to help achieve denser interconnects, which translates into greater power optimization and an improved signal propagation within the component. The die-to-wafer (D2W) direct hybrid-bonding process using copper/oxide mix interfaces has been identified by major microelectronic industrial companies as essential for the success of future logic and memory stacks, thanks to its promising low interconnection pitch and known good die (KGD) selection capabilities.

Last year, CEA-Leti demonstrated D2W hybrid bonding with 10µm interconnection pitch and a simple process adapted from its wafer-to-wafer (W2W) expertise. The latest major advances in die-bonding-alignment capability, through its collaboration with SET, paves the way to reach 5µm interconnection pitch. Exploratory work on the process of reducing the alignment to <1µm has already been demonstrated in the development of a self-assembly process. In November 2020, the institute demonstrated proof-of-concept of the KGD approach, compatible with direct hybrid bonding, that involves selecting high-topography tested chips (>2µm) and transferring them to direct bonding that tolerates a maximum topography of 10nm. This was made possible thanks to researchers' deep expertise in planarization.

Learn more:

Die to Wafer Direct Hybrid Bonding Demonstration with High Alignment Accuracy and Electrical Yields, Jouve A. et al., 3DIC 2019

Towards a Complete Direct Hybrid Bonding D2W Integration Flow: Known-Good-Dies and Die Planarization Modules Development, E. Bourjot et al., 3DIC 2019

Self-Assembly Process for 3D Die-to-Wafer using Direct Bonding: A Step Forward Toward Process Automatisation, Jouve A. et al, 2019 IEEE 69th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, USA, 2019, pp. 225-234, doi: 10.1109/ECTC.2019.00041.

Known Good Dies (KGD) strategies compatible with Die-To-Wafer Direct Hybrid bonding **CEA-Leti:** E. Bourjot, P. Stewart, N. Bresson, L. Sanchez, C. Castan, G. Mauguen, Y. Exbrayat, V. Balan, F. Fournel, S.Cheramy, P. Vivet SET Corporation: N.Raynaud, P.Metzger

CEA-Leti Announces Collaboration with Intel to Advance Chip Design Through Cutting-Edge 3D Packaging Technologies.

Part of this work was been developed in the frame of IRT Nanoelec.

...to greater flexibility

Beyond power and interconnections, 3D technology also allows for the manufacture of more efficient, thinner, and lighter microprocessors. In addition, by implementing multiple heterogeneous solutions in a single package, chip companies benefit from considerable flexibility, allowing them to mix and match technology blocks with IP and integrate memory and input/output (IO) technologies within the same component.
A good example of this is the collaboration between CEA-Leti and Intel. Their research focuses on the assembly of smaller chips, the optimization of interconnection technologies between the different elements of microprocessors, and on new bonding technologies and stacking for 3D integrated circuits (3D ICs), in particular for the realization of HPC applications, by leveraging advanced 3D packaging technologies (Figure 1).

Enabling high-performance processors to power exascale computing

Computing performance has grown exponentially in recent decades. This has led to HPC opening the door to new horizons and allowing for the resolution of extremely complex problems that require processing vast amounts of data. Supercomputers will soon achieve exascale-level computing performance: 1018 flops, or one-billion-billion floating-point operations per second.

Learn more:

How 3D Integration Technologies Enable Advanced Compute Node for Exascale-Level High Performance Computing? D. Dutoit et al. IEDM 2020

Die-to-Wafer 3D Interconnections Operating at Sub-Kelvin Temperatures for Quantum Computation; C. Thomas and al. ESTC 2020.

French Team on Route Towards an Interposer Prototype for Quantum and Control Chips Integration at Very Low Temperature (CEA-Leti Press Release, Nov. 2020)

Part of this work was developed in the frame of IRT Nanoelec.

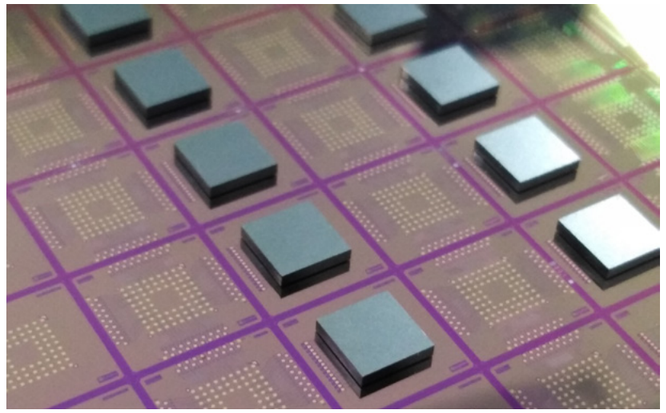

Figure 2: Intermediate silicon prototype of multichip module with flip chipped AsGa Devices

However, in the context of HPC, the integration of greater computing capacities with generic cores or dedicated accelerators for AI applications comes with significant challenges. Manufacturing yield and costs remains the main hurdle. 3D technology appears as a clear alternative to More than Moore, offering a matrix, and modular and robust architecture.

3D integration and quantum computing

In 2019, CEA-Leti developed INTACT, a proof-of-concept integrating 96-core architecture comprising six chiplets (FDSOI 28nm node) 3D-stacked on an active silicon interposer (CMOS 65nm node) (Figure 2). Following this achievement in the HPC domain, similar architectures are envisioned for quantum computation to vastly improve performance and speed. A team of scientists from CEA-Leti, CEA-List, and the Néel Institute at the National Center for Scientific Research (CNRS) designed the first prototype interposer in 2020.

The interposers' primary purpose is to accommodate and connect quantum chips containing qubits and control chips used to address and read the qubits (two-level storage units for quantum computing using the same approach as for HPC requirements). Known as QuIC3, which stands for quantum integrated circuits with CryoCMOS, this prototype demonstrator is an important step towards the realization of a complete quantum computing system.

CoolCube™: About CEA-Leti's monolithic 3D technology

Since 2016, CEA-Leti has extended its 3D integration roadmap with its CoolCube® technology in which stacked FDSOI transistors are interconnected with pattern alignment accurate to the nanometer, which is what makes all the difference compared to 2D technology. This also allows an increase in the density of the components without reducing their dimensions. As an extension of high-density 3D Cu-Cu/hybrid bonding chip-to-wafer/wafer-to-wafer technologies, CoolCube™ enables stacking active layers of transistors in the third dimension, while coping with thermal budgets that do not degrade the performance of transistors or metal interconnects. CEA-Leti works on various 3D very large scale integration (VLSI) advanced concepts, which have broad applications in low-power mobile devices and other IC platforms.

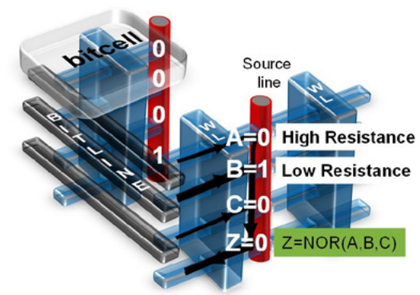

Figure 3: My Cube concept: highly parallel in-memory computing.

In June 2020, in an FDSOI CMOS processing breakthrough, CEA-Leti pushed fabrication thermal-process boundaries down to 500°C for CMOS integration, while showing strong performance gains especially in p-type metal-oxide-semiconductor (PMOS) logic devices. The 500°C threshold is important because in 3D monolithic technologies (also called 3D sequential), fabricating the upper-level transistors at higher temperatures than that, can damage the metal interconnects and the silicide of the bottom-level transistors. Using CEA-Leti's CoolCube® low-temperature process for top-level devices prevents deterioration of bottom-level transistors.

CEA-Leti has recently exploited the CoolCube® technology to increase the density of resistive memory arrays by fabricating monolithically integrated multiple one-transistor/one-resistor (1T1R) structures, reducing the cell size by 1.5x with respect to planar 1T1R. The proposed 3D monolithically integrated multiple 1T1R cells have been combined with multilevel cell programming to further enhance memory density.

Improving 3D technology also means imagining and designing new 3D architectures. Developed by S. Barraud et al. at CEA-Leti in collaboration with the University of Aix-Marseille, a new 3D memory cube architecture composed of nanosheet gate-all-around (GAA) transistors stacked vertically makes it possible to overcome the limitation in the size of cells imposed by a conventional transistor. This new type of stacking, developed for advanced CMOS, has excellent 3D integration scalability (Figure 3).

CEA-Leti and its partners have demonstrated along the year's relevance of 3D architecture for high performance applications by leveraging a wide range of technologies, from direct hybrid bonding, sequential 3D integration, to silicon interposer. The future is vertical.

Learn more:

CEA-Leti Scientists Demonstrate CMOS Device Fabrication at 500°C, Paving the Way to High-Performance 3D Monolithic CMOS Integration

3D RRAMs with Gate-All-Around Stacked Nanosheet Transistors for In-Memory-Computing, S. Barraud et al, IEDM 2020

High-Density Multi-Level-Cell 3D Sequentially Integrated 1T1R RRAM Array for Neural Networks, E. Esmanhotto et al, IEDM 2020

3D Sequential Integration: Opportunities, Breakthroughs and Challenges IEDM 2020 Short Course Session 1 by Claire Beranger-Fenouillet

This work was partly supported by the European Union's Horizon 2020 research and innovation program under Grant Agreement No. 820048 (ERC My Cube); No. 295970 (ANDANTE), No. 826655(TEMPO), and No. 871371 (MeMScales).

The Big Squeeze – Why OSATs Need to Work Smarter

By Danielle Baptiste, VP and GM, Software, Onto Innovation

Analysts are projecting strong growth in advanced packaging, with a compound annual growth rate (CAGR) through 2026 approaching 7% across the segment; much higher for certain high-end technologies, including 3D stacking, embedded die, and fan-out. Outsourced assembly and test (OSAT) firms, which package finished die manufactured by independent device manufacturers (IDM) and foundries, will be challenged by the complexity of the advanced packaging processes and will face stiff competition, in many cases from their own customers. If they are to thrive, or perhaps just survive, they will need to embrace smarter manufacturing approaches.

Gathering process data is key

The historical division between front-end device manufacturing and back-end packaging/testing is the result of their vastly different cost structures and process complexity. The relative simplicity of the back-end process led OSATs to compete primarily on price, seeking always to minimize costs and maximize volume. Simple processes were simple to control. The acquisition, storage, and analysis of process data were costs to be avoided wherever possible. Advanced packaging processes have introduced a host of new variables that must be controlled to ensure process yield and product reliability. Process data is no longer a cost to be avoided but should be considered an essential asset to be leveraged to maximize profitability.

Meanwhile, as they accommodate increasingly complex processes, OSATs confront encroachment in their markets by sophisticated competitors who may also be their customers — IDMs and foundries who have outsourced a significant portion of their production to OSATs but have also maintained their own internal back-end capabilities. Advanced packaging processes have been described as the migration of front-end like processes to traditionally back-end applications. With this evolution, the advantage device manufacturers once had by outsourcing assembly and test to avoid diluting their expertise with low-value processes has greatly diminished. More importantly, these customers-turned-competitors are already comfortable with managing complex processes — they wrote the book. In addition to IDMs and foundries, substrate and printed circuit board (PCB) suppliers, electronic manufacturing services (EMS), original design manufacturers (ODM), and others see the opportunity presented by the significant growth forecasted for advanced packaging.

Smart manufacturing needs broad, deep data

Data is the life blood of smarter manufacturing — acquiring it, storing it, organizing it, analyzing it, sharing it. Without leveraging it you are not just blind in the competitive

Continued on page 65

The People Who Make DBI Possible

A Conversation with Xperi's Hybrid Bonding Team

By Françoise von Trapp

In the world of heterogeneous integration, hybrid bonding — and in particular, Direct Bond Interconnect (DBI®) is quickly becoming the preferred permanent bonding path for forming high-density interconnects in a multitude of applications, from image sensors and MEMS devices, and most recently memory — with RF devices and logic poised for take-off. Since it was first conceived in the mid-80s by Paul Enquist, Q.Y. Tong, and Gill Fountain in the labs at Research Triangle Institute (RTI), DBI has proven to be a game-changer for its elegance and simplicity. It creates a dielectric-to-dielectric bond, and the interconnection is formed by metal-to-metal contact through a low temperature process.

But DBI is so much more than its technology. The people behind this revolutionary and disruptive process are the real story — from those who first developed it, to those who joined the technology team along the way, and the business and marketing minds who brought it to commercialization. While the technology ownership has changed hands — its original company, Ziptronix, was acquired by Xperi in 2015, and is now part of Xperi's Invensas semiconductor technology portfolio — the people who first developed and patented the technology are still very much involved. In this exclusive interview, we asked the core DBI team to tell their stories about being part of the DBI journey, the roles they play, the challenges they've overcome, and what the future holds.

The Early Days

Paul Enquist and Gill Fountain

Before Ziptronix existed, Paul Enquist and Gill Fountain (pictured below) were already at work developing this hybrid bonding solution at RTI. It began with the ZiBond® direct bonding process and then led to the discovery of forming the interconnect, which became DBI.

As Gill tells it, the RTI team was working on a multichip module (MCM) for a customer that involved integrating memory, a processor, and FPGA on top of DRAM. The complexity of the project had them "tearing their hair out" for over a year. Through the ZiBond process of bonding chips on the face of the DRAM and then using a redistribution layer (RDL) to form the interconnect, Gill and Tong discovered a better approach to RDL. By using plating technology, specifically — chemical mechanical polishing (CMP), they could achieve a flatness that allowed the Ni and oxide to not only bond but form an interconnect.

"Everyone thought it was a stunt. Nobody believed the process was reproducible. But it was!" he said. "Later we discovered we could do it with copper." And so, by happy coincidence, DBI was born.

"Bonding was what we first built the company on," says Gill, "The holy grail was to have the connection automatically come with the bonding by taking a dielectric and metal surface, polish it flat and make a connection. It was amazing! That was really something for a group of guys from a research background. It was quite a development."

Paul says it was a matter of being at the right place at the right time, and it was enough to spark the interest of investors. So, after years of building the technology behind both ZiBond and DBI at RTI, it was time to spin out a start-up.

"We got the first round of venture capital funding, took a handful of engineers, and turned them into entrepreneurs," said Paul. While it took 10-15 years to come to fruition, which was longer than anyone wanted, Paul says it aligns with how long things take in the semiconductor industry. "Founders like Gill have put decades into this. It's been quite a ride," he added.

Gill says the first big break for DBI came when Raytheon showed interest. "They saw that DBI would give them not just bonding, but connectivity at the pitch they needed, and they were sold," he said, "It was a huge break that led to the first technology transfer. We demonstrated we had something real and not just a science fair project. It was a real technology that could have a powerful impact on the industry."

"It's one thing when you use your technology, but when other people use it, that's a great proof point," said Paul. "That was the first stage of adoption."

Figuring out how to perform DBI using Cu, so that it could be aligned with standard semiconductor processes was another important milestone, noted Paul. Then the CMOS image sensor market took off, driven by smartphones, and with it a need to scale pixels using bonding technologies. DBI made it possible to make connections between the two wafers. Sony licensed the technology, which was another big break for DBI.

The Acquisition

Craig Mitchell

Craig Mitchell, (pictured below) President of Invensas, a wholly owned subsidiary of Xperi, says he started watching DBI back in 2003.

"I was keeping an eye on the technology to see if it could scale and be applied to a high-volume market," he explained. "The Ziptronix team proved that out by working with some pretty big semiconductor manufacturing companies. We could see that this was where the industry was headed and that there would be a need for this type of bonding and interconnect technology that would allow the industry to continue to scale."

Bringing Ziptronix and Invensas together at the right time meant they could continue building on the foundation that Ziptronix had established. "It's been continuously exciting," he said.

"We were a start-up for 15 years, and I didn't think we'd get out of it," said Gill. "When Invensas came along, it was a game-changer for all of us. We thought it would never happen. It seems like you just have to hang in there until the time is right." Becoming part of Invensas opened up the opportunity to expand on many more levels, such as incorporating TSVs into the technology.

The Transfer to Invensas

Guilian Gao and Cyprian Uzoh

Guilian Gao, distinguished engineer and Cyprian Uzoh, principal engineer, were also involved early in the acquisition process, performing due diligence to evaluate the fundamentals of ZiBond and DBI.

Before joining the DBI team, Guilian (pictured right with Laura Mirkarimi) worked on the 3D team at Invensas, working on through-silicon via (TSV) integration with solder cap and microbumps, examining the technology fundamentals. Because of this work, she knew it would be hard to scale processes below 40µm. DBI provided a scalable interconnect alternative, and she was very excited about its possibilities.

Cyprian, a research scientist at IBM, was invited by Bel Haba to join Xperi to work on TSVs in 2010. Cyprian (pictured below) drew on his expertise in Cu interconnect technology to review the full patent portfolio, mapping and studying the core patent claims for evidence of use. Cyprian's inventions, such as bottom-up Cu fill for TSVs, are the core foundation of modern chip interconnection technology. If anyone could tell if this process was going places, it was him.

Guilian was the first person to touch DBI on its journey from Ziptronix in Raleigh, North Carolina to Invensas, in San Jose. She worked with Gill to put together the technology transfer package for both ZiBond and DBI. The situation was a little unusual, as Gill couldn't travel because of an ankle injury. "I was in my home talking to Guilian on the phone and using WebEx, so it was interesting," he recalls.

"We had lots of daily conference calls because my starting point was low," said Guilian. "I came from a board assembly background, so it was a steep learning curve for me, but Gill was a very patient and excellent teacher."

The Next Era of DBI Development

Laura Mirkarimi and Tom Workman

A veteran of Invensas who had left in 2015 for a position at Zeiss Group, Laura Mirkarimi rejoined Invensas as VP of 3D Portfolio and Technology in February of 2016 specifically to lead the R&D development for DBI.

"That was my first introduction to DBI and I saw the incredible potential of this clever platform technology," she said. "It's not a single point solution, it's a platform toolkit from which to design features into products. Once you have it in your toolkit, it becomes pervasive."

Her team works together to address fundamental challenges in DBI, and how to proliferate the technology across multiple applications. This includes internal development and partnerships to ensure the silicon supply chain is ready for the technology.

Together, the team brought up the new Class 1000 assembly lab cleanroom, the level of clean needed for DBI processes. They added back-end-of line equipment including CMP capabilities and various metrology tools. Every piece of equipment was new and some of it was custom built by "Gill Co." (the code name for home-built by Gill Fountain, because the necessary tools had yet to be built by suppliers.)

"We brought it up and qualified it. That is how I learned to walk with DBI," said Guillian. " I have been in the lab for the past 5 years, doing something new each day. It is never boring. I am a bit like the glue in the 3D group. I know a little bit of everything to be dangerous in the lab. I am a co-inventor on many DBI related patents. I am also a messenger of the technology through publications."

Through the evaluation process, Cyprian learned what improvements are needed for manufacturing processes and lower costs. He continues conducting experiments and develop new methods, chemical formulas, new equipment designs, and more. For example, he developed a custom tool to meet the stringent cleaning requirements for die-to-wafer DBI® Ultra processes.

"I was excited about the patents. Cleaning tools needed to be redesigned, so we brought it in-house to make the technology work and reduce the cost," said Cyprian. His work and pilot operations have led to extensive patent filings.

Laura explained that it was important to understand customer pain points that could be solved by integrating DBI into the process flow. Using solder interconnect and everything to do with it was an ongoing issue that could be solved with DBI.

"We've had excellent input from top tier manufacturers that reinforce where the technology can go. It took a significant engineering effort to get to an HVM-worthy process with a keen understanding on the fundamental physics," she said. "We started early on with die-to-wafer, but the tools weren't ready in the semiconductor space. It takes time to get the infrastructure in place and then take off."

Tom Workman is a principal engineer, who joined the development team in 2017, was also drawn by the opportunity to work on DBI. "At Intel, I worked on the C4 bumping process. DBI interested me enough to get me to join Xperi," he said. "It seemed to be something that takes C4 to the ultimate conclusion — bonding two chips together without intermediary bumping or metallization. It's exciting to take a genius idea, dig in, and optimize it for HVM."

Tom works closely with the tool vendors. "Three years ago, it was a tough sell to bonding tool companies to meet the specifications for DBI. But now, it's the exact opposite," he said. "These companies are coming to us with test specifications from device companies asking for cleanliness requirements. We've become a resource for equipment manufacturers. We have some great partnerships with equipment suppliers where there is motivation on both sides."

Building the Business

Rick McClellan

On the business side, Rick McClellan, VP of Business Development, says it's the people at both Ziptronix and Xperi who made it the success it is today. For him, one of the most instrumental people for helping him early on was Kathy Cook, who was his business development colleague first at Ziptronix, and then again at Xperi. Kathy also joined Invensas as part of the Ziptronix acquisition. She has now moved on to another Xperi spin-in — Perceive, where she is VP of Business Development.

"When I first joined Ziptronix in 2013, I was effectively joined at the hip with Paul and Kathy. And I can't tell you how much they helped me learn and understand the basics, so I could go out and bring the messaging in front of these companies," says Rick.

After the acquisition, he left to join SK hynix for a spell and then was hired by Craig to work at Xperi in 2017. He was excited about joining an even bigger team of talented people.

What Rick enjoys most is working with Paul, Tom, and Laura on customer engagement. When Tom presented recent findings at IMAPS DPC in March 2020, Rick watched from the background (pictured below left with Tom). "He was bombarded by questions. It was exciting to see everyone's enthusiasm for this technology," he said. "We've got an entire generation of engineers that are thinking and designing in 3D and that's what has them excited."

Another story he likes to tell is when he joined Laura and Tom on a visit from a tier-one memory company to the Xperi R&D facility in San Jose. These potential customers were still doubtful about a room temperature bond. "Laura and Tom arranged an entire demo in the cleanroom. Tom went through 60 die-to-wafer placements in real-time and handed them the wafer," he recalled. "Everyone in the group tried to push the die off the wafer that Tom had just bonded at room temperature. The die wouldn't budge. and you should have seen the look on their faces. Needless to say, they are a licensee today."

Marketing the DBI and DBI Ultra Brand

Abul Nuruzzman

Abul Nuruzzman who is currently VP of Product Marketing, joined the DBI team in 2015 shortly after the acquisition of Ziptronix and has lived through the merger with DTS and rebrand as Xperi.

“Helping to drive the market success of DBI, as well as oversee the introduction of DBI Ultra was exciting,” said Abul. “We launched die-to-wafer hybrid bonding to the market earlier than anyone, including major semiconductor companies like TSMC, Intel, who followed with similar die to wafer market announcements.”

Abul is fascinated by the technology, especially how these micro and nanoscale processes can have such a big impact at the device and system level. He enjoys worked with the technology team to craft the DBI story and creating process flow diagrams and models. "It's one of

the best jobs I've ever had," he says.

Abul says It was a bit of marketing challenge in the beginning, because the Ziptronix brand was so well known. But because the foundational technology brand has remained consistent despite the change in the corporate brand, Abul says the DBI brand story remained stable. "New things happen, things change, but the essence of hybrid bonding and the education process to communicate its core values and performance doesn't change," said Abul.

The key, Craig says, is to maintain consistency with the technology brands. "We invest in those brands. Sometimes the corporate brand evolves, but it's important to maintain the product brands," he explained.

Abul noted that the product line branding posed its own subset of challenges, as the technology itself evolved. For example, a completely different set of challenges had to be solved to develop the die-to-wafer version of DBI. As such, the team believed it deserved its own brand and came up with the DBI Ultra name.

Big Breaks and Plot Twists

"From the commercial perspective, licensing a company like Sony was a massive milestone," said Craig. "It set the stage for broader industry to evaluate its potential and apply it to their technology and product roadmaps." A more recent milestone was licensing the technology to SK hynix for its memory products, as well as seeing it adopted into other high-volume markets beyond image sensors.

"I'm excited to see where things go next," says Craig. "As DBI finds its way into bigger markets and proliferates into other applications, it opens up the door for the entire ecosystem to embrace the technology. The more people involved, the more we'll see it applied in other applications. There are exciting milestones still to come."

"Moore's Law scaling is so expensive. Only a few foundries are continuing to do it. One way to compensate for that is 3D stacking and scaling," noted Abul. "That's why DBI is getting attention in the memory and logic space for high-performance computing."

"There have been many plot twists over the years," said Paul. "While the fundamental technology remains stable, lots of things have changed. While investors, customers, business models have changed, the core technology has not. For example, during the Y2K euphoria, investors were throwing money at it and we were lining up customers. Then the bubble burst and we had to adjust the business plan and the story. But the technology got us through."

"I don't think the industry fully appreciate the significance of DBI as a room-temperature process," says Cyprian. He says when he was at IBM working on Watson, they were bonding silicon on insulator (SOI) wafers at 1200°C. "We couldn't imagine doing that at 200°C. It never occurred to us that we could bond at a low temperature."

Laura says it's easy to forget how they felt the first time they looked at DBI. "What amazed me was the simplicity around it and the problems it solved," she recalls. "It looked so clever. The fact that the bond happens at room temperature and then is heated to enhance the interconnect is beautiful. The physics works." She added that she could see why companies would want this technology, especially after all the money spent on advanced packaging technologies to come up with an MCM.

"If you can control things to take advantage of bonding at room temperature, you can really start to think about true heterogeneous integration," she said.

What the Future Holds

"We have so much flexibility with ZiBond, DBI, and DBI Ultra," said Laura. "We're going to see so much innovation and new architectures in the memory/logic space. By developing DBI Ultra, we have the ability to do high volume manufacturing for true 3D integration."

"Because of this technology, I believe in about 10- or 15-years demand for things like underfill and solder will go down," says Cyprian. "I believe in the future we'll be doing ZiBond at 100°C, which means we can have polymer materials that are high performance, but because of temperature issues haven't been able to use them."

"I see ZiBond and DBI as the tools in the 3D integration toolbox that the industry will rely on for decades to come," said Craig. "We're just at the early stages of DBI adoption. We see it in image sensors already — we'll see it in RF and memory. In logic, the combination of logic and memory, and the disaggregation of devices, DBI can be that core enabling technology that is pervasive throughout the semiconductor space and allows us to scale performance, functionality, cost, power, leveraging the existing infrastructure."

Conclusion

So, there you have it: the DBI story through the eyes of the people who are making it happen. What I loved most about this conversation is that every single person is passionate about the technology, from those who conceived it to those who joined Xperi just for the opportunity to work on DBI. It's because of all of them that it is succeeding. Technologies don't just happen. It takes people to discover them, realize their potential, and push them to succeed. Paul, Gill, Craig, Guilian, Cyprian, Laura, Tom, Rick, and Abul, - I can't wait to see where you take this technology next.

Rising from the Ashes: StratEdge Corporation's Recent Rocky History

Figure 1. The fire and smoke damage

By Casey Krawiec, StratEdge Corporation

Since its founding in 1992, StratEdge has moved its factory a couple of times. Its recent move from Sorrento Mesa, in San Diego, to nearby Santee, California, was not by choice. The president of StratEdge, Tim Going, received a most unpleasant call while on a business trip in November 2018. The fire chief told him that StratEdge was on fire. It is not the call you want to receive. It's like driving your car and realizing you have a flat tire and need to pull over to fix it. But this sinking feeling in the gut is a hundred times worse. The fire originated somewhere in the plating area, which included nickel and gold plating lines. The burning plastics and chemicals created plumes of caustic smoke that essentially gutted the building and destroyed almost all of the electronics within the equipment (Figure 1).

A Stormy Past

StratEdge has always been a nimble company, making adjustments in strategy or product offerings to stay competitive in the semiconductor packaging and assembly business. It's an industry where the only constant seems to be change.

The company has weathered storms in the past. When it was founded and became StratEdge, it was owned by a Venture Capitalist (VC). With its patented designs, StratEdge rode the telecom boom in the 1990s with highly successful products used in very small aperture terminals (VSATs), internet infrastructure, and automated test equipment (ATE). But like so many other companies, it was brought to its knees by the telecom bust in the early 2000s.

"I remember going to the Optical Fiber Conference (OFC) in Atlanta in 2003," Jerry Carter, senior technologist and 28-year employee reminisced. "It was like a ghost town. The aisles were empty because no one attended. The saddest thing was many of the booth sites were vacant because the companies either went bankrupt or decided to skip the show to save money on travel expenses."

After attending the IEEE MTT-S International Microwave Symposium just a few weeks later, the VC decided to pull the plug. The portfolio of companies in the fund were bleeding cash, and despite a relatively healthy backlog of orders, without VC funding, StratEdge became insolvent. The plan of being

Figure 2. StratEdge's Class 1000 cleanroom and class 100 work areas

Figure 3. Belt furnaces for package manufacturing

Figure 4. New StratEdge headquarters in Santee, California.

acquired at a handsome price, like so many dotcoms, had become an impossible dream, and the company had to be revamped.

Back and Better than Ever

Fast forward to today. The 2018 factory fire had a couple of silver linings. The storeroom was on the opposite side of the building from the fire and the inventory was protected in vacuum-sealed bags, so no finished goods were lost. The company also had good insurance, which allowed for replacement equipment to be purchased. And finally, the employees remained loyal while the rebuilding effort took place. Most of StratEdge's employees have been with the company for over fifteen years.

Although a daunting task, rebuilding the company practically from scratch had some benefits. StratEdge had been working with Palomar Technologies for several years on perfecting gold-tin (AuSn) die attachment of chips, with a concentrated focus on gallium nitride (GaN) devices. Die attachment is the process of attaching a device to a tab or heat spreader, package, or another die. StratEdge developed a proprietary AuSn eutectic die attach technique that, in conjunction with its leaded laminate (LL) packages with CMC bases, was found to achieve superior thermal dissipation. The Palomar 3880, a fully automated die bonder, was purchased and installed along with other sophisticated precision equipment in a new Class 1000 cleanroom, which includes Class 100 work areas with ESD control for performing sensitive operations (Figure 2).

Even though StratEdge is mostly known for its high-performance, high-power packages made from post-fired ceramic and molded ceramic materials, the company has provided microelectronic assembly services since the late 1990s. The influx of new, state-of-the-art assembly equipment increased throughput for the assembly of high-frequency and high-speed monolithic microwave integrated circuit (MMIC) devices, along with passive components including some with 50-ohm lines. This new automated equipment and proprietary die-attach method performs precise eutectic, epoxy die attachment, and wire bonding to ensure short, consistent loop lengths and heights for the most optimal electrical performance. The company assembles packages and lids manufactured by StratEdge, as well as customer-furnished packages and boards. The flexibility of the equipment and skill of its operators enables StratEdge to accommodate the numerous needs of its customers.

As mentioned, StratEdge has designed and manufactured packages for compound semiconductors since its beginning. Some of the belt furnaces used to produce molded ceramic packages were more than 40 years old. Amazingly, some of the ancient furnaces survived the fire. The replacement furnaces are state-of-the-art, with multiple sensors that allow more precise control of the various heating zones within the furnace (Figure 3). Since their installation, yields have steadily improved. With the new larger facility and better equipment, StratEdge's capacity for building ceramic and molded ceramic packages in support of 5G infrastructure has increased. The packages, most often used to protect high-power laterally-diffused metal-oxide semiconductors (LDMOS), gallium arsenide (GaAs), silicon carbide (SiC), and GaN devices, match standard outlines developed to support cellular base stations. Run rates in excess of 100,000 packages are being accommodated.

"As a result of the fire, StratEdge moved into a new facility in 2019 where we continue to design, manufacture, and provide assembly services for a complete line of post-fired ceramic, low-cost molded ceramic, and ceramic QFN packages, some of which operate from DC to 63+ GHz," said Tim Going, president and CEO of StratEdge. "Although the process of rebuilding has certainly had its challenges, it's positioned us to meet the increasing demands for 5G equipment and specialized defense and commercial applications, including radar, communications, avionics, and customer-premises equipment (CPE)." (Figure 4.)

Conclusion

The old saying about when life hands you lemons, make lemonade, is true. The fire facilitated an upgrade of the entire company. StratEdge is better positioned to support its customers, including those with aerospace and military applications, than ever before. The advanced packaging lines and microelectronic assembly services, combined with electrical and environmental test capabilities and design services, have well-positioned the company to support its customers in the various industries in which they participate.

The Importance of Sustainability in Semiconductor Manufacturing

By Dean Freeman, FTMA

Since the Kyoto Protocol was adopted in 1997 and ratified in 2005, sustainability has been a much-discussed topic. In 2015-2016 with the adoption of the Paris Agreement, which is an update to the Kyoto Protocol, sustainability discussions and actions started to move forward with much more vigor. Even though the US administration in office from 2016-2020 withdrew from the agreement due to the amount the United States was financing it, as well as concerns about jobs for coal and oil companies, many US companies embraced the Paris Agreement and set-in place sustainability targets that are published either in annual reports or in a corporate social responsibility report (CSR). Based on the number of corporate announcements regarding the increased use of renewable energy to replace coal, oil, and natural gas as energy sources, this renewed effort is very visible. Moreover, with continued improvements in battery storage, the US continues to increase its use of renewables as a viable energy source.

Semiconductor Sustainability Efforts

Years ago, SEMI spearheaded environmental safety and health (ESH) safety standards for the industry, as well as restriction of hazardous substances (RoHS) efforts, and organized a green manufacturing committee. SEMI also helped coordinate efforts to reduced ozone-depleting gasses, back when the semiconductor industry used and released ozone-depleting gasses into the atmosphere. Techniques were developed to either find alternative gasses for use in the production facilities or methods to reduce the level of gasses released into the atmosphere.

At virtual SEMICON West 2020, SEMI focused several keynotes on sustainability, featuring first former Vice President Al Gore, followed by Gary Dickerson, of Applied Materials (AMAT) who laid out the company's sustainability program for the future. According to Dickerson, AMAT will have 100% renewable energy sourcing in the U.S. by 2022 and worldwide by 2030, and a 50% reduction in Scope 1 and 2 carbon emissions by 2030. AMAT has several power purchase agreements where they expect to achieve 100% renewable sourcing in the United States and 73% worldwide by 2022. Dickerson also announced plans for a more sustainable supply chain, both from an energy and water perspective, as well as a materials responsibility perspective.

While the Applied Materials press engine made a big announcement at SEMICON West, other companies in the semiconductor industry have been focused on sustainability for many years as well, some with a great deal of success. Lam Research has been publishing sustainability reports since 2013. The company set five-year goals in 2015 and achieved those targets in 2019.[1]

Many semiconductor equipment companies such as Lam, ASML, Tokyo Electron (TEL), and AMAT are using the United Nations Sustainable Development Goals to help them set targets for future sustainability, as well as other social needs like diversity, hunger, and caring for the environment in other ways than just eliminating greenhouse gasses (Figure 1).[2]

Most semiconductor equipment companies appear to be taking sustainability seriously and have programs to improve renewable power utilization, as well as to determine how to reduce power consumption and water usage in the equipment that they sell to semiconductor manufacturers. The companies that have been surveyed to date are also exploring how to reduce greenhouse emissions from gases other than CO_2. Two companies that have had concerted efforts without as much press as Applied Materials are ASML, which is a recent addition to the 2020 Dow Jones Sustainability Indices (DJSI), and TEL, which has already made the DJSI list. The Dow Jones Sustainability World Index tracks the performance of the top 10% of the 2,500 largest companies in the S&P Global Broad Market Index℠ that lead the field in terms of sustainability. 79 semiconductor companies were invited to participate in the survey.[3]

Semiconductor Companies are Leading the Way

From a semiconductor company perspective, Intel has been focused on sustainability efforts since before 2000 with efforts to conserve water at its New Mexico facility. In Intel's 2020 Corporate Responsibility at Intel executive summary, the company reports it has saved 44 billion gallons of water in the past decade, along with 37 billion KWH of green

Figure 1: In September 2015, 193 member states of the United Nations adopted 17 new Sustainable Development Goals (SDGs) to make our world more prosperous, inclusive, sustainable, and resilient. Lam recognizes the importance of these goals and the roles businesses play in achieving them. Lam is committed to aligning its programs and initiatives and do its part toward achieving these global goals. (Image source: Lam Research 2019 CSR Report)

Figure 2: Intel's 2020 sustainability goal results summary. (Source: Intel CSR report 2019-20 executive summary.[4])

power. By 2025 Intel expects to restore 100% of its water use.[4]

While not solely one of the key drivers in the semiconductor equipment company's efforts to jump on board the sustainability train, Intel has had a significant impact in moving sustainability forward. When most companies initiate a sustainability effort, they also incorporate their supply chain into the effort. Intel would not have been able to successfully reduce water consumption at Rio Rancho and worldwide without the participation of its key equipment vendors. In 2012, Intel introduced its Program to Accelerate Supplier Sustainability (PASS). The company completes on-site audits for its top 75 suppliers with assessments on 300 factors. In 2019 Intel aimed to have 90% of its suppliers in PASS meeting advanced expectations (Figure 2). These programs are likely part of a catalyst for many companies in the semiconductor manufacturing industry to have initiated their CSR programs, as most appear to have started the programs in the 2013-2014 time.

Intel is not the only semiconductor company to have a strong focus on sustainability. TSMC, the industry's largest foundry, also has embarked on a significant sustainable effort. TSMC's sustainable goal for 2030 is to supply 25% of the power consumed by its fabrication plants from renewable energy, and 100% for other facilities' power consumption. In July 2020, TSMC's power purchasing agreements for renewable energy totaled 1.2 GW, and the company also officially passed the qualification to become the world's first semiconductor company to join the RE100.

As a whole, semiconductor companies are making a concerted effort in the sustainability area. In the October 12, 2020, Wall Street Journal's top 100 most sustainable companies, three semiconductor companies, and one equipment company are listed:

- 31 Texas Instruments
- 48 Intel
- 66 Ebara
- 71 ST Microelectronics

This is a fairly significant achievement considering the WSJ looked at over 5500 companies in their study.[5]

As mentioned above, the Dow Jones Sustainability Index (DJSI) monitors many companies worldwide using a rigorous methodology. Fifty-eight semiconductor-related companies were assessed in 2020. Of those 58 companies, seven made the world-wide list, others made regional listing. ASML Holding NV was added in 2020 to the worldwide list. Other companies on the world-wide list are TSMC, UMC, Win Semiconductor, ASE Technology Holding Co., Infineon Technologies AG, and ST Microelectronics NV.

Companies that received a regional listing are Texas Instruments, SK Hynix, TEL, Micron, Nvidia, On-Semiconductor, and Intel.

To get an apples-to-apples assessment of how companies are performing against one another from a sustainability perspective, it would be beneficial for them to participate with an organization that has a consistent methodology and ranking such as DJSI.

ASE is a DJSI World Leader

ASE has been on the DJSI as a world leader for the past five years — a considerable accomplishment, considering the other companies on the world-wide list are from Taiwan.[6] ASE has increased renewable electricity use in 2019 by 29% over 2018 and seven of its manufacturing sites have achieved over 100% renewable electricity usage. Water usage is down by 9% over 2018. ASE also participates in a reforestation project to assist in the mitigation of greenhouse gasses. Since 2017, 27 hectares of land and 40,000 seedlings have been planted.

From the semiconductor industries' participation in the DJSI, as well as the focus on corporate social responsibility in companies' corporate reporting, it is apparent that semiconductor companies have taken their role in improving sustainability seriously. Even to the point where companies such as Intel are looking at how they can reduce the power consumption in processors, and equipment companies consider how to reduce water and power usage in process equipment. As semiconductor companies continue to set goals and plan it will be interesting to see how they continue to drive the needle in improving sustainability.

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Fan Out Panel Level Packaging Takes Off

By Ralph Zoberbier, Roland Rettenmeier, Allan Jaunzens, Evatec

Fanout (FO) packaging is one of the key growing segments in advanced packaging, with high adoption rates and strong technology advantages offering a strong pathway moving forward to support industry roadmaps. The nature of reconstituted substrates is now enabling FO packaging on panels too. Fan out packaging is no longer limited to the silicon wafer format, opening up a whole new range of possibilities. OEMs are aggressively driving their contract manufacturers to utilize these new substrate sizes and packaging processes to leverage cost savings. Qualifying power management ICs (PMICs) and developing the next generation of chiplet packages are interesting challenges that lay ahead now that high performance, fab-compatible (full SECS/GEM and OHT integration, etc.) panel solutions are commercially available.

The first developments for panel level equipment and process solutions were undertaken by the supply chain five years ago, and since that time the first R&D and pilot lines were established. These lines evolved into pilot production in 2020, and in 2021 we will see early adopters finally move into high volume manufacturing with a wider range of products. As reported by Yole Développement, leading companies like Samsung, Nepes, and Powertech International (PTI) have publicly announced their

What Does PLP Mean for Seed Layers?

Seed layer deposition is one of the most critical process steps in manufacturing vertical and horizontal interconnects. At the panel level, seed layer deposition must deliver high performance degas, etch, and sputter deposition processes as well managed substrate temperature throughout the whole process to ensure low contact resistance (Rc) and excellent adhesion of the seed layers prior to downstream processing. (litho, electroplating, etc.).

Step 1:

Repeatable and reliable outgassing of organic substrates

Degassing is an important first step in ensuring good bond strength for the seed layer. Industry solutions so far have included both atmospheric and vacuum approaches. Diffusion of volatile components from the bulk material to the surface is driven by temperature and time.

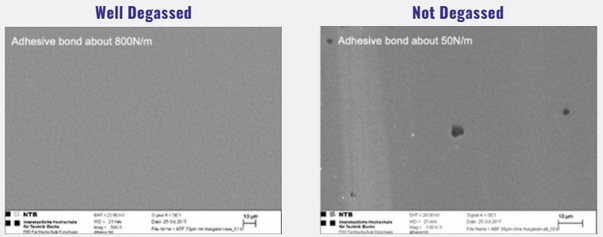

Figure 1: Large difference in film quality and adhesive strength for films deposited on Ajinomoto Build-up Film (ABF) GY50 substrates without or with prior substrate degas. (Images courtesy of NTB, Buchs: Substrate material: ABF GY 50, 20nm SiO2 equivalent etc. 100nm Ti, 300nm Cu, electroplating, structuring and milling of coupons prior to peel tests according to IPC standards).

Desorption is driven by the concentration gradient, which is the same whether desorption takes place under vacuum or in atmosphere. However, the advantage in atmosphere is that the concentration gradient can always be kept high if a laminar flow of inert gas is applied while under vacuum, the degassing of the volatile components has to take place by less efficient molecular diffusion. So far, it looks like atmospheric technology where a batch of substrates are simultaneously degassed in multiple heated slots with nitrogen laminar flow will be the winner for organic substrates (e.g. AMC, ABF, PID, PI, etc.).

Features favoring atmospheric degas technology include fast and precise temperature control of substrates (conductive heating), emissivity independent temperature control (no overheating and no local hot spots), and transport of volatile compounds away from the substrates (no re-contamination)

SEM images in Figure 1 illustrates film quality on ABF GY50 substrates with and without prior degassing. Without proper degassing the films can end up with defects such as voids or holes. In peel testing according to IPC standards, adhesive bond strength was measured at 800N/m for well degassed substrates but only 50N/m for equivalent processes omitting the degas step.

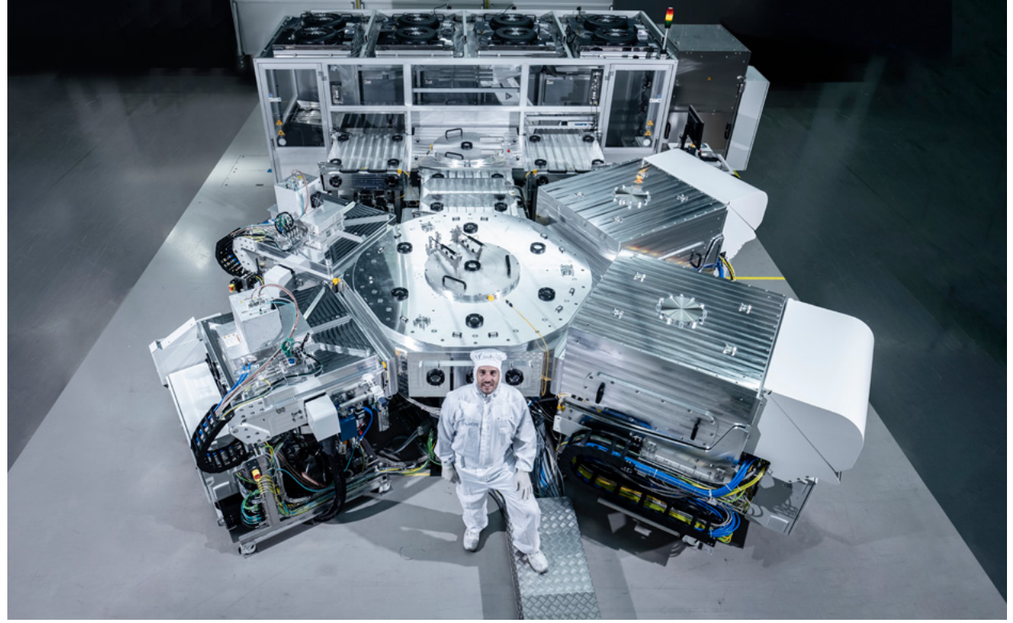

Figure 3: Fully automated cluster tool for panel sizes of 600x600mm integrating degas, etch and deposition process modules

readiness. Others like ASE Group, Amkor Technology, and newcomers like ESWIN are coming to the end of their final technology qualifications as 2020 closes and are ready to make the next big step by including panel packaging into their product offerings. All this can be considered as the first wave of panel level packaging.

Next generation developments in systems in package (SiP) or solutions for AI and high-performance computing (HPC) applications will also then push the industry towards very large package bodies. This second wave will also require panel level packaging (PLP) technologies as current wafer dimensions and shape will severely limit the overall substrate utilization and be detrimental to overall cost of ownership. Of course, technical process performance, handling capabilities, and semiconductor like quality must be proven. Missing industry norms and standardization were an issue in bringing the technology to market over the last few years but finally, we at least now

Step 2:

Etching processes — perfectly tuned for large area panel processing

Removing native oxides and preparing the substrates' interface are the major reasons for etching in advanced packaging. Low Rc and superior adhesion of the sputtered seed layer are the results.

Key requirements for high process repeatability and yield are high etch uniformity over large areas with low edge exclusion and particle avoidance. Substrate damage must be avoided by controlling plasma densities and ion bombardment, while etch powers/rates also need to be managed to remain within thermal budget.

Etch uniformity results on a panel size of 600m x 600m using a capacitively coupled plasma (CCP) source are shown in Figure 2. The achievable uniformities of <10% fall within the specifications demanded by process developers and processing with a static panel addresses the key concerns of reducing risk of particle generation.

Some process technologies such as laser via descum or

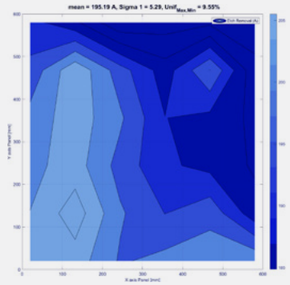

Figure 2: Etch uniformity over 600x600mm panels is better than 10% with an edge exclusion of 20mm

forming vertical interconnects will also require combinations of physical and chemical etch (CHF3, C3F8, CF4, O2, N2+H2, Ar+H2, etc.)

Step 3: Sputter deposition - Superior seed layer adhesion and uniformity

Just like for the etch process, key performance specifications for overall process yield include high deposition uniformity with low edge exclusion and avoidance of particles.

Deposition uniformity results for the required Ti and Cu layers are shown for panel sizes of 600mm x 600mm in Figure 3. In this case, rotating target sputter technology (Figure 4) also enables processing static panels to reduce risk of particle contamination while still achieving the required deposition uniformities.

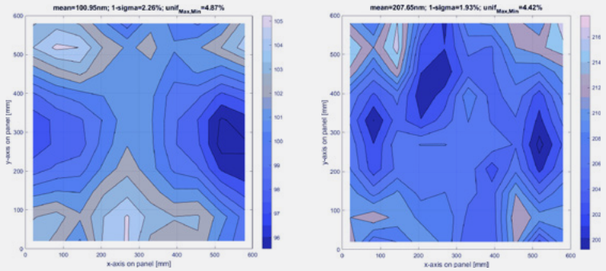

Figure 3: Deposition uniformities over 600x600mm panels better than 5% on titanium and copper layers with an edge exclusion of 20mm

Figure 4. Rotating cathode sputter technology delivers excellent uniformity over large areas

see consolidated panel sizes for 600x600mm and 510x515mm in the industry (Figure 1).

Market Outlook

Establishing PLP manufacturing lines does require investment in dedicated panel equipment for temporary bonding, pick-and-place, molding, grinding/polishing, sputtering, resist lamination, lithography, electro plating, and etching. Utilizing 300mm equipment might then be reasonable for back-end-of-line (BEOL) processes such as testing and dicing. Nevertheless, PLP certainly offers the potential for lower cost of ownership due to the larger substrate area and better economical manufacturing of bigger packages because of better material utilization. Many analysts have looked at the merits in moving from wafer to PLP packaging in more detail. It is certainly clear that with a bigger size of substrate the substrate cost portion per package should see a significant reduction due to economies of scale.

Within a typical FO manufacturing process, the redistribution layer (RDL) cost is considered one of the key contributors at around 40%. The largest costs for the RDL itself come from material costs like photo dielectrics and plated Cu, followed by Capex costs for lithography and metallization equipment. In moving from wafer to panel, the contribution of material costs is expected to stay at a similar level, so cost reductions will be sought in equipment that simply processes larger substrates with more packages at the same time. Multiplying the output by a factor of three or more, but still achieving the same level of process performance on 500mm panels as on 300mm wafers, is the biggest argument for PLP. Rectangular substrates are also preferred over round when it comes to material utilization — especially with bigger packages as illustrated in Figure 2.

Process technologies like lithography, seed layer deposition and electrolytic plating play a key role in enabling cost effective, reliable high-volume manufacturing on large substrates. After a long period of investment in hardware and process developments, the equipment industry is now able to provide tailored equipment solutions.

Sophisticated technologies might continue to drive device technology forward at the wafer level, but the baseline expectation is that performance at panel level will keep up to match whatever is achieved on wafer scale.

Panel Solutions Are Ready Now

Figure 3 shows an example of commercially available SEMI compatible cluster tool designed for panel sizes up to 650x650mm.

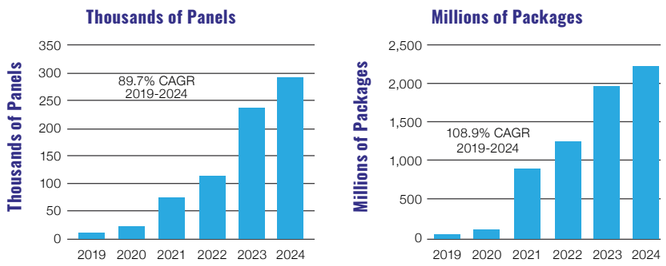

Figure 1: Market forecast for low density FO Panel Demand (Courtesy of TechSearch International)

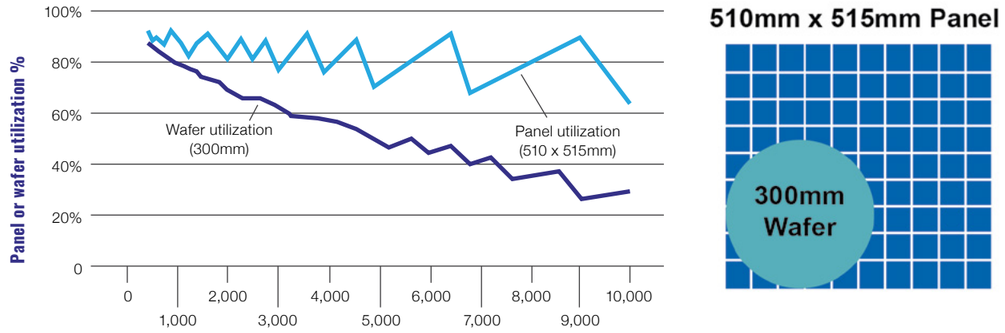

Figure 2: Advantages of advanced packaging on panel: The economic cost advantages of manufacturing on panel level get bigger with die size (As presented by Intel at IMAPS 2020)

We believe It's going to be an exciting time for the advanced packaging industry and panel processing technology as capacities ramp in the years to come, but if you don't believe us why not listen to what the industry experts say. The situation was well summarized by Boris Hsieh, CEO of PTI inc. in a recent interview with Digitimes:

"In terms of advanced packaging technology, TSMC now offers the largest InFO capacity in the world and Samsung Electronics also has its own advanced packaging solutions, but PTI now focuses on FOPLP technology. We are continuing negotiations with potential clients over the FOPLP backend services.

If InFO and FOPLP are both suitable for packaging some types of ICs, the latter can offer more-cost-effective production as panels can be cut into subpanels that will involve simplified process and competitive cost structure to help clients save production cost. And we are targeting leading vendors of networking chips as potential clients for our FOPLP services, and it will not be impossible for us to serve even vendors of GPUs and handset APs in the future."

Die-to-Wafer Bonding Steps into the Spotlight on a Heterogeneous Integration Stage

By Dr. Thomas Uhrmann, EV Group

The semiconductor industry is currently undergoing the most radical change in its history. Many new applications such as artificial intelligence (AI), augmented/virtual reality and autonomous driving require enormous computing power with processors optimized specifically for each application. At the same time, development cycles are becoming shorter, costs for new chip designs are rising exponentially, and in many cases, yields are declining. All of these aspects can only be tackled if the principles of the entire semiconductor manufacturing process are changed.

While 2D transistor scaling is still important, the rising costs and complexity associated with scaling have driven the semiconductor industry to turn to 3D integration and heterogeneous integration — the manufacturing, assembly and packaging of multiple different components or dies with different feature sizes and materials onto a single device or package — to increase performance on new device generations supporting these new applications.

This migration to advanced packaging as a leading driver of innovation began with the transition from monolithic to die-level systems, such as newly released smartphone application processors, which combine individual components such as the processor, memory, and AI/neural components using advanced packaging. This transformation will only accelerate in the coming years with the further miniaturization of these components from dies to chiplets, thus enabling a much more precise and individual mapping of customer and application requirements.

	Co-D2W	DP-D2W
Transfer Method	Collective Die Transfer by Reconstituted Carrier	Direct Placement of Activated Dies using Flip Chip Bonder
Pros	• Proven technology • Die activation and cleaning equivalent to W2W hybrid bonding • Oxide management • Rework on carrier feasible	• Versatile method • Die thickness invariant
Cons	• Error propagation of D2W + W2W alignment • Cost of carrier prep, utilization and clean • Die thickness needs to be in narrow range	• Bonding interface needs to be touched • Die handling, especially for multi-die stacks such as SRAM, DRAM • Particle management during die placement

Table 1: Hybrid die-to-wafer bonding approaches for heterogeneous integration

Chiplets and Hybrid Bonding

The ability to split large chips that are several hundred square millimeters into smaller parts can result in better yield, thus saving costs. Furthermore, only those chiplets requiring the latest-generation-node lithography have to be produced with that technology, whereas the remaining chiplets can be manufactured with older-generation (and less costly) lithography processes. Thus, the complexities and innovations of semiconductor manufacturing are increasingly shifting into advanced packaging, which in turn makes flexible hybrid bonding technologies increasingly important.

Wafer-to-wafer (W2W) hybrid bonding, which involves stacking and electrically connecting wafers from different production lines, is a central process in heterogeneous integration and has a proven track record of success for CMOS image

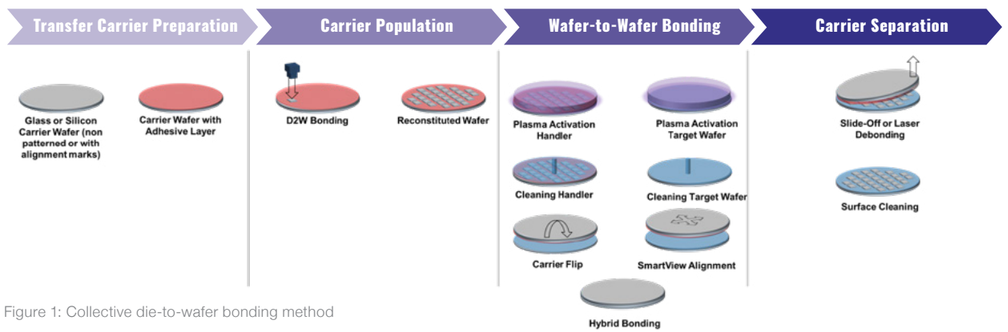

Figure 1: Collective die-to-wafer bonding method

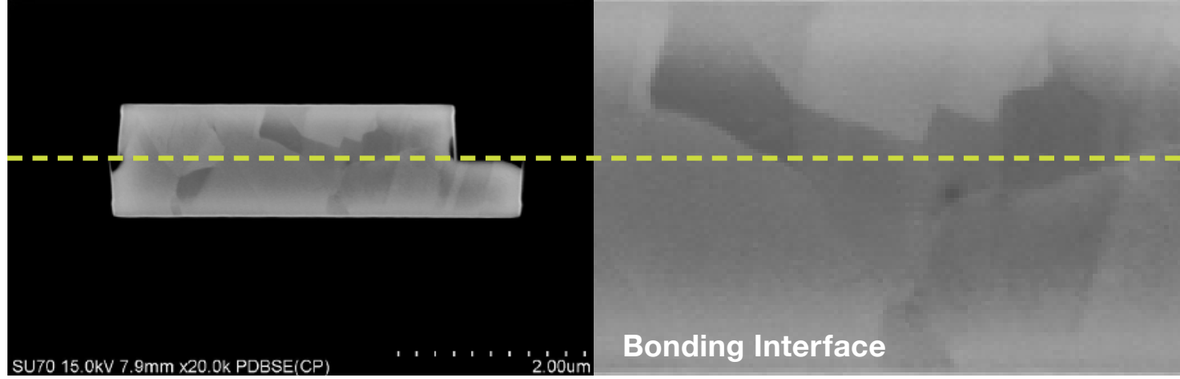

Figure 2: TEM cross section images of die to wafer bonded interfaces using hybrid bonding

sensors and various memory and logic technologies. However, since many chiplets are not necessarily the same size, a die-to-wafer (D2W) hybrid bonding approach may be a more practical option. There are several different D2W bonding approaches being considered for heterogeneous integration, each with different advantages and disadvantages as shown in Table 1. Determining which approach is best suited to a given application depends on several factors such as die size, die thickness, and total stack height as well as interface considerations such as contact design and density.

Collective Die-to-Wafer Bonding

One hybrid D2W bonding method that has already been implemented in volume production for the past few years for applications such as silicon photonics is collective die-to-wafer (Co-D2W) bonding. In Co-D2W bonding, singulated dies are transferred via a carrier wafer to the final wafer and bonded collectively in a single process step. The manufacturing flow for the Co-D2W bonding process is shown in Figure 1 and consists of four major segments: carrier preparation, carrier population, wafer bonding (temporary and permanent), and carrier separation.

Prior to the initial wafer dicing process, the wafer is coated with a protection layer to preserve the bonding interface quality during the dicing and pick-and-place processes as the bonding interface is orientated face-up on the dicing tape. The protection layer material can be a commercially available positive resist and/or any other protection layer that fulfills the specification of the dicing method used and can be subsequently completely removed using a solvent- or water-based cleaning process. The spin coating of the protection layer onto wafers with low topography can be performed using an EVG150 automated coating tool. For wafers with a topography that is greater than 5µm, spray coating can be performed using the same equipment.

To temporarily place the die on the collective die carrier using a pick-and-place D2W bonder and lock in their position during the cleaning, die preparation, and transfer process, the carrier wafer is coated with a commercially available temporary bonding material. The type of temporary bonding adhesive that is used depends on the post-processing steps and can be deposited on carrier substrates using the EVG850TB temporary bonder. Different metrology systems can be used during the carrier preparation process, such as the EVG40NT to measure die placement accuracy and the EVG50 to evaluate the incoming die height variation die-to-die surface planarity and the adhesive thickness.

The diced dies coated with the protection layer are placed with the bonding surface facing up on the collective die carrier to allow removal of the protection layer from the die surface. This removal can be accomplished using an EVG320 automated cleaning system using solvent-based and/or water-based cleaning chemistries.

In preparation for the hybrid bonding process itself, plasma activation in combination with deionized water-based wafer cleaning is used for substrate preparation on both the collective die carrier and target wafers. The carrier wafer is then flipped and aligned with the target wafer using an EVG SmartView NT optical aligner. Next, the dies on the carrier wafer are bonded with the target wafer using a GEMINI FB automated fusion wafer bonding system. Separating the collective die carrier from the transferred dies can then be accomplished using laser or thermal slide/lift-off debonding.

A recent publication highlighting this method demonstrated <2µm placement accuracy and high die transfer rate using currently available wafer bonding and debonding, die bonding, metrology and cleaning process equipment.[1]

Figure 2 shows the transmission electron microscope cross-section images of the transferred dies after hybrid bonding. A closed bond line with Cu grains grown over the bonded interface could be demonstrated after subsequent thermal annealing. The Cu grain growth over the bonded interface indicates a high bonding quality. Further alignment improvements are expected with the next generation of die bonders, enabling the process flow to achieve well below 1µm overall die alignment accuracy.

Direct Placement Die-to-Wafer Bonding

Another hybrid D2W bonding approach that is beginning to be implemented for heterogeneous integration applications is direct placement die-to-wafer (DP-D2W) bonding whereby the dies are transferred to the final wafer one at a time using a pick-and-place flip-chip bonder. Figure 3 shows the manufacturing flow for the DP-D2W bonding process, which consists of three major segments: carrier population, die clean and activation, and direct placement flip chip.

The DP-D2W bonding process flow begins much in the same way as the Co-D2W bonding process flow, with singulated dies added face up to a carrier wafer. Even though DP-D2W offers higher flexibility compared to Co-D2W, especially in terms of multi-die stacking for high bandwidth memory, the challenges in cleanliness and activation are the same as with any fusion bonding technique. In order to transport the wafers from the back-end grinding and dicing steps to a front-end clean hybrid bonding step, the dies often require repopulation on a dedicated cleaning carrier wafer. The carrier wafer then undergoes plasma activation and cleaning. However, instead of bonding the carrier wafer to the target wafer, the dies are bonded to the target wafer one by one using a pick-and-place flip-chip bonder.

The die cleaning step is a crucial part of the overall process flow that demands a dedicated tool for cleaning and activation. The recently introduced EVG320D2W has been designed as a highly flexible die preparation and activation system that features a universal hardware/software interface to enable seamless integration with third-party pick-and-place die bonding systems. It also can operate as a stand-alone system depending on integration and line balancing requirements. The system incorporates EVG's advanced cleaning and plasma activation technology, which is available across its W2W fusion and hybrid bonding platforms and has been proven in hundreds of installed modules worldwide. It also features an integrated metrology module that provides direct feedback to the die bonder on critical process parameters, such as die placement accuracy and die-height information as well as post-bond metrology, for improved process control.

An Incubator for New Heterogeneous Integration Concepts

To determine the best bonding method for their respective devices, manufacturers must put together extensive development projects that not only take into account the wafer bonding equipment itself, but also the materials involved (such as photoresists and adhesives for temporary and permanent bonding), as well as related equipment and processes (such as wafer cleaning, carrier handling, die bonding, etc.). Extensive process expertise is a must, while having access to the latest-generation technologies is also key. However, since these systems are often already in production use at the customer's site, they may not be easily accessible for R&D or experiments.

To address these challenges, EVG established the Heterogeneous Integration Competence Center™ (HICC), which assists customers in leveraging EVG process solutions and expertise to enable new and enhanced products and applications driven by advances in system integration and packaging. The basic idea for the foundation of the HICC is to make the barriers for development as low as possible to customers and to offer EVG as an incubator for new ideas. Through the HICC, EVG can assist in accelerating technology development, minimizing risk, and developing differentiating technologies and products through heterogeneous integration and advanced packaging all while guaranteeing the highest IP protection standards that are required for working on pre-release products.

Summary

D2W hybrid bonding is an enabling process to accelerate the deployment of 3D/heterogeneous integration and bring about new generations of devices with high bandwidth, high performance, and low power consumption. While the infrastructure for D2W hybrid bonding is still evolving, new process solutions and collaborations across the supply chain are on the rise and will play an essential role in creating best known methods of D2W hybrid bonding.

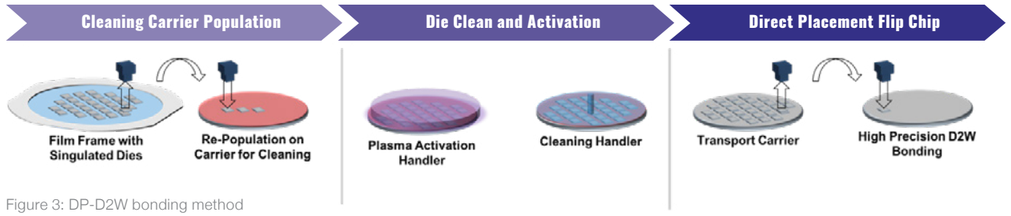

Figure 3: DP-D2W bonding method

Acknowledgement

The author wishes to thank Jürgen Burggraf and Mariana Pires of EV Group for their assistance with the development of this article, as well as thank IRT Nanoelec and CEA-Leti for providing the substrates used in the CoD2W bonding demonstration cited in this article.

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The Future is Heterogeneous Integration continued from 17

of many electronic components, subsystems, and electronics products.

ASE has developed and offers a wide portfolio of Si-level integration technology solutions, from low- to high-density chiplet integration including flip-chip multi-chip-module (FC-MCM), fanout chip-on-substrate (FOCoS), and 3D IC. The advanced FOCoS technology can provide short die-to-die connection and high interconnections (10,000s), redistribution layers (RDL) with 2µm line/space, and up to four layers for chip-first and chip-last packaging processes. It produces a lower-cost solution with improved electrical performance compared to a 2.5D Si interposer solution due to the elimination of Si through silicon via (TSV) processes and reduced insertion loss. ASE is evolving this advanced packaging platform to meet application demands for HPC and AI/ML applications.

A Smarter, Healthier, More Efficient Future

Semiconductor applications do exist everywhere in our daily lives today. Engineers constantly face significant challenges, albeit very different from the challenges faced by engineers in the 1960s. One cannot but be deeply motivated by a speech delivered by the former President of United States, John F. Kennedy on September 12, 1962, "We choose to go to the moon in this decade and do the other things, not because they are easy, but because they are hard because that goal will serve to organize and measure the best of our energies and skills, because that challenge is one that we are willing to accept, one we are unwilling to postpone, and one which we intend to win, and the others, too."

Looking further into 2021 and beyond, key developments in packaging that create higher performance systems and utilize less power will be deployed. System performance will continue the pace of the Moore's Law era, albeit in a different way than with the previous total reliance on semiconductor chip lithography and SoC integration. There is tremendous optimism that innovations in the IC packaging industry will continue on a heterogeneous integration journey. Discovery, creativity, innovation, and very importantly, collaboration - will enable applications that make our world smarter, healthier, and more efficient. It is our hope to leave it in an infinitely far better place for future generations to live, work, play, and communicate.

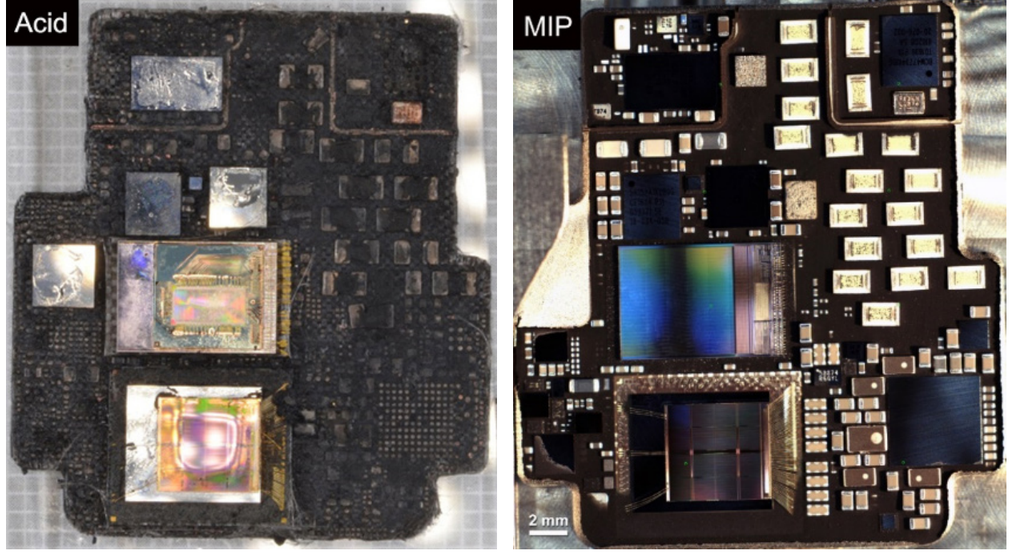


Figure 1. A 26mmx29mm SiP module after acid decapsulation (left) and after MIP decapsulation (right)

Artifact-free Decapsulation of 2.5D and 3D Semiconductor Packages with Atmospheric Pressure Microwave Induced Plasma for True Root Cause Analysis

By Lea Heusinger-Jonda and Jiaqi Tang, Ph.D.

As semiconductor devices are subject to increasingly higher quality and reliability standards, extensive measures must be taken to ensure these standards are met. At the same time, new highly integrated, complex packaging solutions – including a variety of new materials and structures – are being adopted to achieve the economic and performance advantages that were previously met with silicon scaling. These factors call for the use of highly advanced tools to analyze potential failures, which often require physical access to the die. Obtaining unambiguous results in failure analysis strongly depends on the quality of sample preparation, such as selective removal of the encapsulant material while preserving the bond wires, re-distribution metal, bond pads, passivation, die, and the original failure sites.

Due to the stacking structure and relatively small, package-to-die size ratio, the decapsulation of complex 3D stacked-die packages appears to be very challenging when using conventional techniques involving acids or carbon tetrafluoride (CF4) based reactive ion etch (RIE) systems. The latter two techniques have intrinsic limitations, which are especially apparent in advanced packages that include 3D structures.

Conventional acid decapsulation can easily damage the top layer die and bond wires due to overexposure in acid, while the middle and bottom layer structures remain unexposed. It is also quite challenging to preserve the package perimeter in order to perform further electrical tests in specific test sockets when using acid decapsulation. The image labeled ‘Acid’ in Figure 1 gives an indication of the over-etching and corrosion damage induced by acid decapsulation of a system-in-package (SiP) module.

Using conventional CF4-based RIE decapsulation makes it even more difficult to reach the middle and bottom layer structures due to the thick molding compound layer and stepwise structure. Also, CF4 often causes over-etching damage to the passivation layer and the silicon die, as these materials are readily etched in fluorine plasma. The high energy ion bombardment in the commonly used RIE plasma systems can damage the electrical functionality of the device, preventing further analysis steps. To summarize: The use of acid or CF4-based plasma decapsulation methods can induce damage or alteration of original structures, and possibly introduce corrosion, over-etching and foreign contamination reducing analysis accuracy and confidence levels during root cause failure analysis.[1]

To overcome the limitations of conventional decapsulation techniques and enable artifact-free sample preparation, a fully automatic decapsulation machine has been developed based on

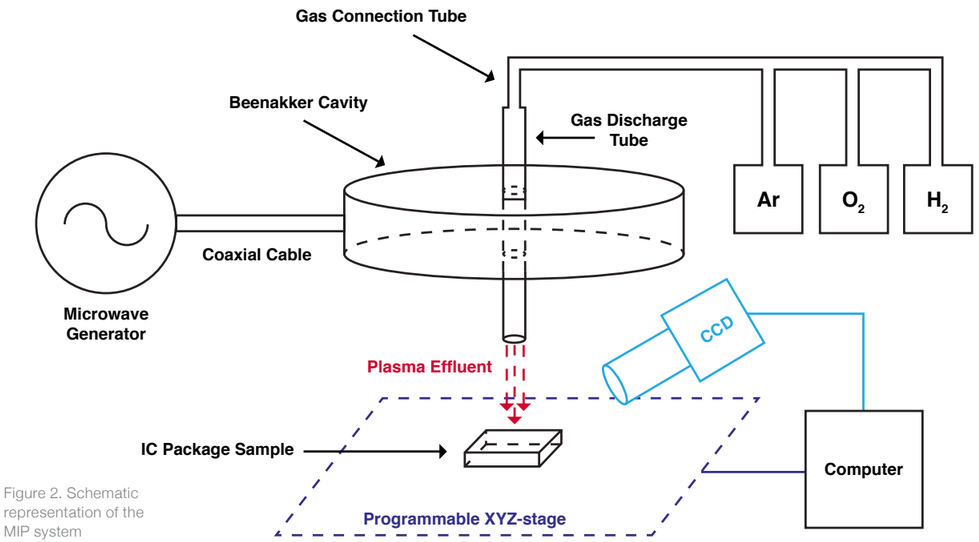


Figure 2. Schematic representation of the MIP system

novel, low-power (P<100W) atmospheric pressure microwave induced plasma (MIP). The highly confined plasma beam of the MIP tool results in a high flux of neutral oxygen radicals in the plasma afterglow, which contributes to the high molding compound etch rate and high etch selectivity of common wire bond materials, such as gold, silver and copper, and Si die. As has been previously reported, the atmospheric pressure oxygen-only MIP etching can achieve high selectivity of mold compound to wire/pad/passivation/die.[2] The absence of ion bombardment and microwave stray fields is crucial to prevent damaging the device inside the package. It has been shown that semiconductor devices remain fully functional after their packages have been decapsulated using the MIP tool.

The MIP tool consists of a low-power microwave generator (2450 MHz), a custom-built Beenakker-type microwave resonant cavity, a gas discharge tube, mass flow controllers, a camera, a programmable XYZ-stage, cleaning unit and drying unit (Figure 2).

The MIP process is carried out in two steps. During the first step, the epoxy in the molding compound is selectively removed by high density oxygen radicals in the MIP effluent beam that are scanned across the sample surface. During the second step, the remaining agglomerate layer of silicon dioxide filler particles is removed in an ultrasonic deionized water bath. This etch-clean-dry cycle is repeated, enabling layer-by-layer removal of epoxy mold compound while the functional components and the original failure sites in the package are preserved.[3]

Figure 3 illustrates the described MIP decapsulation process flow. Sample preparation is not necessarily required prior to MIP processing. However, to optimize the process and reduce overall decapsulation time, it is helpful to remove bulk mold compound above the top wire loops using methods such as laser ablation or milling. Figure 3a shows a package after laser ablation, which is then etched by MIP in Figure 3b, and cleaned in deionized water in Figure 3c to remove the filler particles.[4]

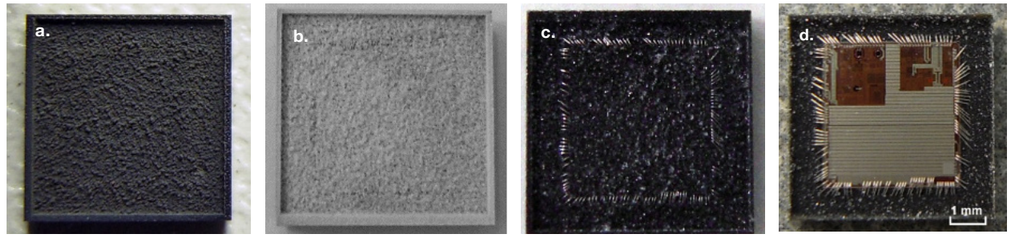


Figure 3. Process flow of the halogen-free MIP decapsulation, showing a) the package surface after laser ablation, b) followed by MIP etching, and c) followed by ultrasonic cleaning in deionized water to remove the SiO2 filler particles. d) fully decapsulated sample

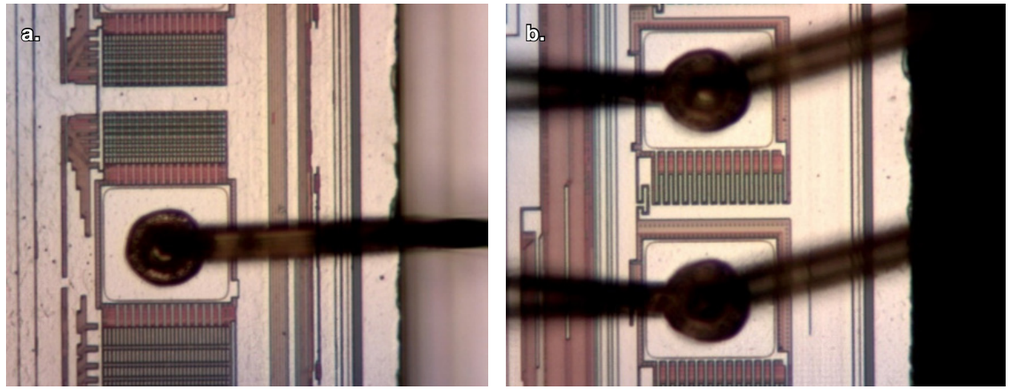


Figure 4. Optical microscope image on the 1st layer (a) and the 2nd layer of flash memory stacked die (b) in the SiP module after MIP decapsulation

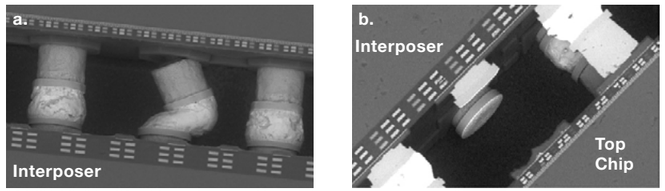
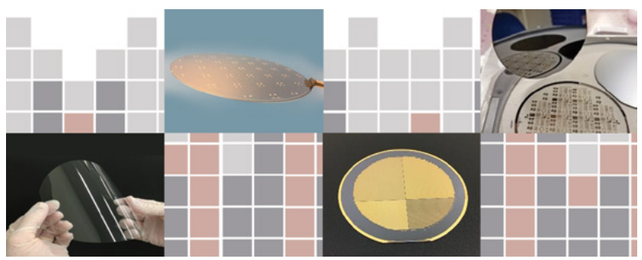


Figure 5. a) MIP processing exposed the first row of µpillars in a cross section and b) MIP process was able to expose the second row into the sample where the first µpillar row was mechanically polished into



The etching chemistry and subsequent high selectivity of the MIP decapsulation process removes the risk of overetching and facilitates the removal of the packaging material while ensuring that the bond wires, bond pads, dies, original structures, and failure sites are preserved in an excellent state. The image labeled MIP in Figure 1 illustrates artifact-free exposure of all active and passive devices in a SiP module using MIP. Figure 4 shows more detailed images of a decapsulated 3D structure on the SiP module.

As part of the MIP tool's continuous application development, focus has recently been placed on 2.5D packages, proving that the MIP process selectively removes organic materials, such as epoxy mold compound, underfill or polyimide, on a die or in-between two dies on the 2.5D package to enable further analysis steps. Cu micro-bump, solder joint, die pad exposure (top down or cross-section exposure) on 2.5D interposer die or 3D NAND dies are areas where MIP shows its unique capabilities compared to conventional decapsulation techniques.

Interposer interconnects, for example, are difficult to expose using conventional decapsulation methods, because the laminate, chip bumps and µbumps would be attacked by wet chemicals. Fluorocarbon-based plasma

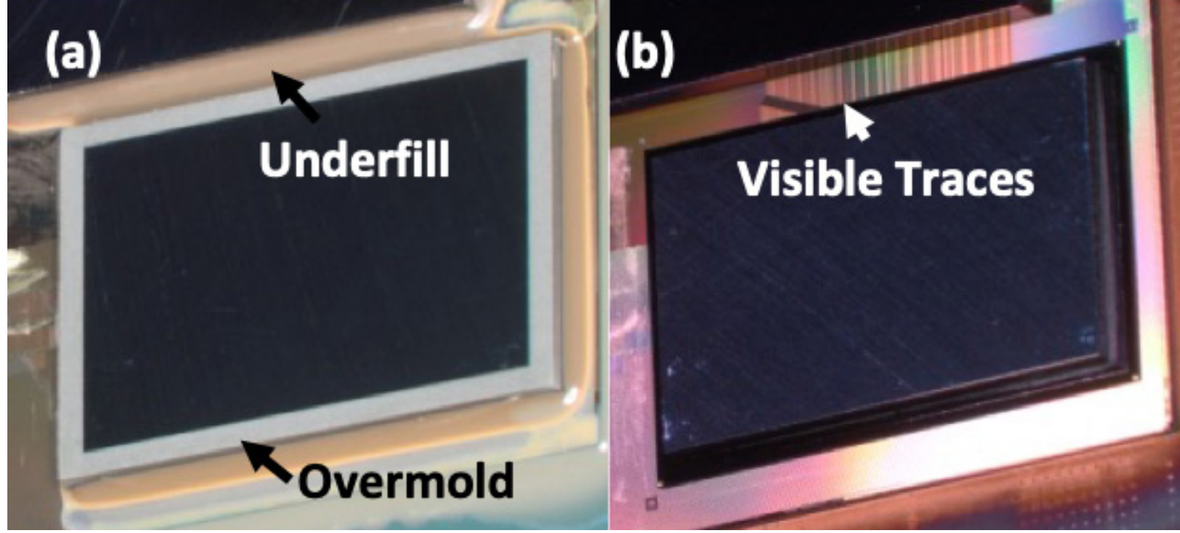


Figure 6. (a) Optical image of High-Bandwidth Memory (HBM) overmold and surrounding underfill. (b) Optical image of HBM after MIP processing has removed the overmold and underfill over the interposer and between the top chips

etchers will attack the passivation, metal layers and chip silicon. Contrary to that, the atmospheric pressure MIP is a highly selective and isotropic process and can expose interposer interconnects while preserving all materials and original failures sites, allowing for subsequent, careful analysis.

Using the atmospheric pressure MIP process to remove underfill over or around 2.5D structures does not alter all other materials on the samples. µBumps can also be cleanly exposed either from the top down or in a cross-section (Figure 5), enabling analysis of defects further into the cross-section, while guaranteeing that no artifacts are induced by the sample preparation.[5]

Removing the packaging material between closely spaced chips on a silicon interposer is quite challenging. MIP's ability to remove the packaging material from these very high aspect ratio spaces allows inspection of the conductive traces in the silicon interposer in this area of high risk of interconnect failure (Figure 6).

The atmospheric pressure MIP system is a unique tool for artifact-free decapsulation to enable undisputable identification of failures. The system's high etching selectivity, speed, and repeatability enables complex advanced packaging decapsulation, ensuring a high success rate of the related failure analyses and reliability investigations.

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Hybrid Bonding Bridges the Technology Gap

By Swati Ramanathan and Stephen Hiebert, KLA Corporation

A Technology Chasm

Until recently, the world of IC fabrication was neatly divided into the distinct stages of front-end and back-end processing, with a large chasm separating them for both process complexity and economic value. The front end has been focused on increased processing or computing power, and achieves this goal using highly complex process technologies to create ever-shrinking technology nodes. Once the devices are built, the wafer moves into the back-end phase, which is focused on connectivity, protection, and assembly. Here, wafers are prepped for assembly into their final packaging by establishing the necessary wiring and connection across devices. Historically, processing in this stage was not as advanced or economically valuable as the front end.

As a result, front-end advances in increasing transistor density and processing speed were pivotal in driving nearly all the improvements in computing — fueling Moore's law. In recent years however, thanks in part to the increased importance of memory in Big Data and AI applications, the semiconductor industry is at a point where processing speed is not the efficiency limiter. The efficiency of the entire finished package is critical and is limited by its least efficient component.

Innovation is not new to the packaging industry, and with packaging processes now directly impacting overall device performance, the pace of invention has gained momentum. It is evident that huge gains can be achieved by increasing bandwidth or the rate at which data is pushed across devices. This shift has accelerated the adoption of some front-end patterning processes [lithography, etch, chemical mechanical planarization (CMP)] to introduce smaller feature sizes and more complex integration in packaging process flows to generate increased connectivity.

As the value of advanced packaging in IC fabrication grows, the technology chasm between front-end and back-end shrinks.

Closing the Gap

As advanced packaging adopts complex processes from the front end, the clear separation that once existed between front-end and back-end wafer processing is starting to blur. This fuzziness is best embodied by packaging technologies like hybrid bonding, which due to its extremely demanding process complexity and small features, uses advanced, almost front-end-like processing (e.g., CMP) to result in improved electrical performance and increased interconnect density.

Hybrid bonding vertically connects die-to-wafers (D2W) or wafers-to-wafers (W2W) (Figure 2) via closely spaced copper pads. While W2W hybrid bonding has been in production for several years in image sensing, there is a strong industry push to expedite the development of D2W hybrid bonding. This development will further enable heterogenous integration, which provides a powerful and flexible means to directly connect die of different functions, sizes, and design rules.

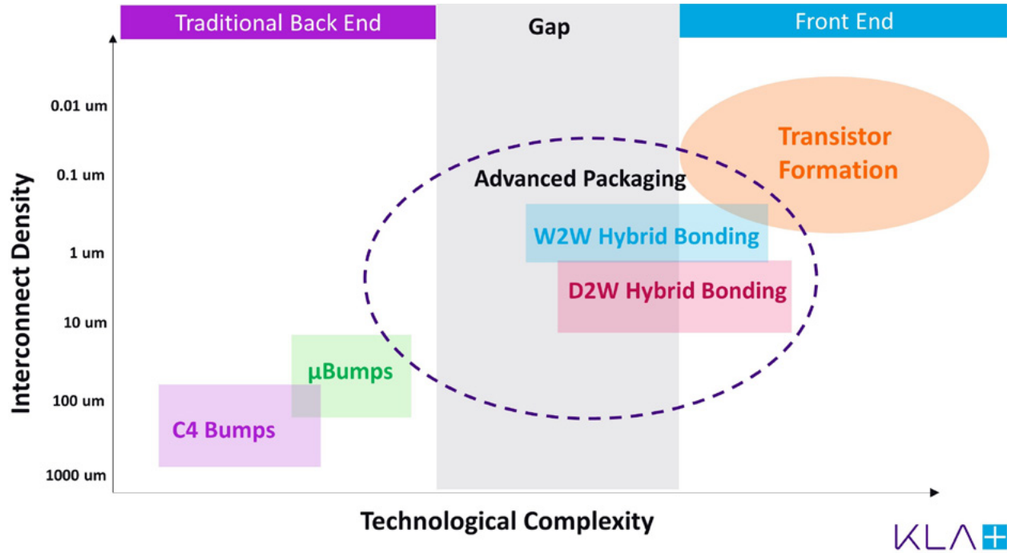

Figure 1: Technology gap between traditional back end and front-end manufacturing phases

The dense copper interconnects associated with hybrid bonding leads to improved electrical performance and bandwidth, while direct die-to-die pad connectivity allows for a lower standoff height and thinner package size. Further, by using pre-inspected, diced known good die (KGD) during the bonding process for applications like 3D stacks in both high bandwidth memory (HBM) and logic, increased yield for the high value package can be realized.

This unrelenting march toward increased efficiency continues to fuel an offshoot of Moore's law; closing the gap between what is considered front end and back end. Additionally, foundries and IDMs already skilled in front-end technology may be quicker to adapt to the high process complexity demanded by hybrid bonding; but OSATs will be working hard to catch up.

Hybrid Bonding Challenges

The use of front-end-like technologies in hybrid bonding is expected to provide huge performance and cost benefits, but not without unique challenges and opportunities for the industry. To keep yields economically favorable, the increased complexity brings about a greater need for metrology, inspection, and testing.

- Shrinking design rules and small copper pad dimensions require precise overlay to ensure pad contact and electrical connectivity
- Surface smoothness, and precise dishing are required, as roughness and imprecise dishing can compromise electrical connectivity

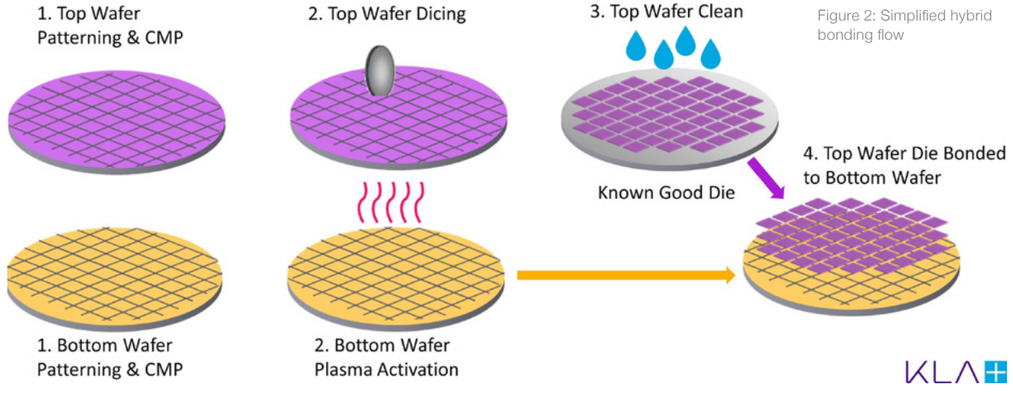

Figure 2: Simplified hybrid bonding flow

- Clean dicing and handling are required to prevent particulation, which can lead to the formation of costly yield killing voids after the bonding step

The successful implementation of D2W hybrid bonding in high volume will require resolution for each of these challenges. To meet alignment requirements, pad-to-pad overlay must be measured through the top die accurately and precisely. The wafer surface profile after damascene pad formation must be measured with sub-nanometer precision to ensure that copper pads meet demanding recess or protrusion requirements. High sensitivity inspection to find all defects early in the process is required to verify that the die surface remains clean for a successful void-free bonding process step.

KLA's Solution

The recently launched Kronos™ 1190 wafer level packaging inspection system is targeted at enabling process development for hybrid bonding, with its high sensitivity darkfield channel for small particle detection and brightfield capability that can detect residue defects. The system can inspect a wide variety of substrate types such as whole wafer, diced wafer on film frame, and reconstituted wafer on carrier to support a broad range of process flows.

In addition to defect inspection, it may be beneficial to use non-mechanical dicing methods like plasma dicing because of much lower particle contamination levels.

KLA's wide range of advanced process control and process-enabling solutions and decades of leadership in front-end process control uniquely position our equipment to address hybrid bonding challenges at a superior cost of ownership.

Novel Approaches to Wafer Handling continued from 18

requires no curing step, and debonds without residue of any kind.

Instead, MESC bonding depends on coulombic attraction between a reusable carrier and the wafer or wafer coupon. Charge stored in an electrode embedded in the carrier induces an opposite charge in the wafer. The attraction between the two maintains the bond until the electrode is discharged. The required charge, a few thousand volts with only a few microamps of current, is far smaller and much more controlled than damaging ESD spikes. Charge monitor (CHARM) wafer testing found no changes attributable to the MESC system.

The bond is robust enough for most mechanical and thermal conditions the wafer might encounter, and is inherently compliant. There is no adhesive between the carrier and the wafer, so differential thermal expansion does not induce stress. High-temperature carriers currently function at temperatures exceeding 450°C and can bond conductive, semi-conductive, and insulating materials. As the wafer expands and contracts, it simply slides on the carrier surface. Bonding and debonding are non-destructive to both the wafer and the carrier; carriers remain reliable for thousands of cycles over many years.

The MESC system works best with smooth, flat, conductive surfaces. It's not limited to such surfaces, though, accommodating most wafers with consistent topography, such as an array of copper studs (the electrostatic bond is not suitable for aqueous processes, as capillary action allows liquid to infiltrate the space between the two surfaces). Reducing the amount of area in contact with the carrier generally reduces the strength of the bond, but varying the amount of electrostatic charge can often compensate for less-than-ideal surface characteristics.

Packaging customer use cases and applications are diversifying at a rapid rate, including reflow, plasma clean, flux clean, flip-chip, and various high-temperature cure techniques. Heterogeneous integration is forcing outsourced semiconductor assembly and test (OSAT) facilities to adopt new production techniques and the adoption of SEMI standards. A lack of standards for device handling and device interfaces has made it challenging for manufacturers to streamline production. There is a movement in the industry to move toward panels that are compatible with the ever-increasing interposer and device-size configurations.

Eshylon's proprietary bonding technology has been proven in both wafer-level and custom-size trays and panel configurations. Carriers can be powered by onboard capacitance or even batteries. With integrated charging stations, carriers can be recharged or powered directly for more demanding process exposure conditions.

Due to the volumes required for large packaging facilities, Eshylon is working on a partnership with a large OEM that currently produces cutting-edge wafer-level and device automated handling equipment. Eshylon has developed a rack mounted charge control module that interfaces with carrier charging units integrated directly into the pick-and-place tooling. This system will communicate directly to the main tool control and will have the ability to control multiple carrier charge units. This handling system will be able to change device bond strength and release on-the-fly, adjusting for varying substrate physical form factors.

Eshylon's electrostatic carrier technology enables customers to run a broader spectrum of products through existing tool sets, reducing production tooling costs and improving overall yields. Taken together, these features make Eshylon Scientific's handling systems for thin wafers and singulated devices a scalable, process compatible alternative to adhesives and tapes.

Fine-Pitch 3D Stacking Technologies for High-performance Heterogeneous Integration and Chiplet-based Architectures continued from 14

by intermetallic compound (IMC) bonding with mechanically stable Cu/Sn Solid-Liquid-InterDiffusion (SLID) interconnects.[18]

To pay more attention to the described fine-pitch stacking concepts and new architectures "between 2D and 3D", the IEEE EPS Technical Committee 3D decided to broaden its objectives from 3DIC and monolithic integration on one side, to non-TSV 3D technologies, chiplet assembly, Si interposer and alternative interposer concepts (including TSV less), on the other side of the fine-pitch interconnect "spectrum".

Visit our website for information on TC 3D/TSV.

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SEMI's Response to COVID-19: Supporting Continuity of Members' Business Operations

By Michael Ciesinski, SEMI

The outbreak of the COVID-19 coronavirus caught most countries and companies off guard and unprepared. Specifically, companies were caught short of personal protection equipment (PPE), along with essential tools, materials, and components to keep manufacturing lines running. Many companies had a business continuity plan (BCP) ready, but all were tested by unanticipated work-from-home (WFH) requirements and adjustments. And, definitions of essential businesses, which could remain open, often varied from region to region and country to country.

A large part of the value SEMI delivers to members comes through connecting people within the microelectronics manufacturing industry — through exhibitions, in-person conferences, global advocacy, standards setting, and workforce development. How could our business model adapt to virtual connectivity and provide the same level of services and information expected by SEMI members?

Launch of the SEMI COVID-19 Communications Team

Ajit Manocha, SEMI's President and CEO, has extensive C-level experience at GlobalFoundries, Spansion, and Philips Semiconductors. He quickly realized the likely and devastating impact of COVID-19 on the global microelectronics manufacturing and design supply chain, and he resolved that SEMI should be an invaluable resource for its members.

Ajit took a page from his manufacturing operations playbook, which directed the leadership team to start each workday with a "morning prayers" meeting where they would review operations and consider how to improve efficiency. He began holding regular early morning meetings with senior SEMI executives to study the latest developments in the crisis, consider members' needs and close on action-items from the previous day.

Based on these meetings, SEMI tasked its technology communities' group and corporate marketing to establish a COVID-19 communications team with the mandate to support member business operations in real time during this unprecedented health and economic disruption. Specifically, the team was to gather coronavirus information, organize it for business purposes, and share it with members.

Various SEMI communities, including Environmental Health & Safety (EHS), Information Technology Leadership (ITL), Fab Owners Alliance (FOA), and Electronic Materials Group (EMG), worked with the COVID-19 communications team to respond to this call for action by gathering and sharing best practices and creating a coronavirus resources webpage as a central hub. The SEMI Global Advocacy team and regional operations teams followed suit in exploring pandemic developments, addressing member needs and contributing content to the COVID-19 communications team.

Supporting Members' Business Operations

The SEMI COVID-19 communications team met frequently between March and November 2020, coinciding with the global reaction to the crisis and up and through wide-scale trials of potential vaccines. These were often twice-weekly sessions encompassing North American, Asian, and European time zones. Output of the SEMI team was prodigious, including:

- Four global webinars, three of which featured pandemic and economic updates and analyses from McKinsey & Co. Subject matter experts, from prestigious organizations such as Wells Fargo Securities and Harvard University's Kennedy School of Government, were also integral elements of the webinars
- Three member surveys to identify pain points, WFH and return-to-work (RTW) policies and strategies, along with key lessons learned
- Dozens of industry meetings to address the supply of PPE, best known safety practices, BCP, state and national regulations, communications infrastructure resiliency, and other business operations topics
- More than 75 blogs and news articles from China, France, Germany, Japan, South Korea, Taiwan, and U.S. featuring member insights, semiconductor industry forecasts, and other relevant information

These meetings and communications continue today and will support SEMI members' needs until such time as the COVID-19 pandemic no longer impacts business operations.

The Value of SEMI's Global Footprint

SEMI operates in seven regions of the world: Americas, China, Europe, Japan, Southeast Asia, South Korea, and Taiwan. This global footprint enabled rapid and insightful communications on the outbreak of the pandemic and steps being taken to ameliorate its effects.

Student attendees at SEMICON China check out the job board in the Workforce Pavilion.

Based on the best local information and in the interests of health and safety, SEMICON Korea, scheduled for February 2020, was cancelled. SEMI postponed SEMICON China from March until June 2020, when it was held successfully as the first major electronics tradeshow and conference in Shanghai, signaling a return to some normalcy. Quickly pivoting to virtual platforms, SEMICON West and SEMICON Southeast Asia were exclusively online, as were key conferences.

In the summer and fall of 2020, SEMI made decisions regarding our remaining roster of exhibitions. SEMICON Taiwan would be our first hybrid event — in-person and virtual. SEMICON Europa was cancelled due to travel restrictions throughout Europe. Also, SEMICON Japan would be virtual. Again, these decisions were made in cooperation with local authorities and in the best interests of the health and safety of our members and their customers.

The SEMI Global Advocacy team played a key role in assuring that the microelectronics industry was considered "essential business" by governments around the world. Starting with letters to governors of more than half of the states in the U.S., this effort soon grew to direct communications from SEMI to the European Union and to government policymakers throughout Asia. It expanded to facilitating essential travel for our members who supply needed equipment, materials and services.

Looking Ahead to 2021

While the world is hopeful about the end of the COVID-19 pandemic, realistically, we know that positive changes and a return to "normalcy" will be gradual. SEMI will continue to support members and the industry at large with resources, updates, and advocacy efforts around the world.

In terms of helping the industry to connect and collaborate at events, SEMI will carefully monitor guidelines in each of our regions for hosting onsite gatherings. We anticipate hosting more hybrid events with a domestic onsite exhibition and a global, virtual version of the technical program to accommodate the differences in situations and travel restrictions by region, along with the full spectrum of stakeholder preferences. Likewise, our various committees and technology communities will host virtual meetings but will seek opportunities to safely host in-person meetings.

The microelectronics industry is poised for continuous growth, thanks to strong fundamentals and technology growth drivers such as artificial intelligence and 5G. The pandemic has sped up aspects of digital transformation, such as remote monitoring of manufacturing equipment and telehealth. SEMI will develop and evolve our initiatives around Smart Manufacturing and Smart MedTech, and other programs and services, to help members uncover new business opportunities emerging from digital transformation. We encourage readers to follow SEMI online and look for ways to get involved.

COVID-19 Stories: How the 3D InCites Community is Navigating the Pandemic

We all had high hopes for 2020. Despite the ongoing Trade War between the US and China, the semiconductor industry was set for growth thanks to high volume drivers like 5G and AI. Then COVID-19 happened, and life changed as the world knew it. We asked our community members to share their stories, both personal and business, of how they are navigating through the pandemic, and what is in store for us in 2021.

Meeting the Needs of a Demanding Semiconductor Market

By Ludo Vandenberk, Trymax Semiconductor

As many of you will agree, 2019 was a very tough year for the semiconductor industry, but with a strong recovery and outlook for 2020-2021 based on order bookings to date and the semiconductor equipment forecast. Before we had time to prepare ourselves for the upcoming demand, there was an unexpected pandemic (COVID-19) affecting our supply chain and equipment manufacturing.

As many European countries went into lockdown randomly over 10 months from March through December, we found that our dual supply chain strategy was mandatory to securing deliveries of the many orders we received and to address the customer's concern for on-time deliveries. The majority of these orders came from our RF-filter (5G), power electronic, and compound semiconductor customers.

At Trymax, we are continuously monitoring the ever-changing climate of the COVID-19 pandemic. We want to assure everyone that our number one priority is the health and safety of our employees, customers, and suppliers. In that respect, from the beginning, Trymax put a dedicated response team in place, which was and still is watching the situation closely.

As part of this, we began implementing measures at a very early stage to secure safety. With the additional measures put in place under our business contingency plans, we have taken the right steps to balance and safeguard the health of our employees and the sustainable production and supply of our products. We believe that we have managed the situation well and therefore do not foresee currently any bigger interruption. The Trymax team would like to extend our gratitude and thank everybody for their contribution in helping our company navigating through this COVID-19 period.

So now the question is what will 2021 bring. At this moment we are all still facing challenges as a result of COVID-19. Together we can remain strong and resilient. Our prospects for 2021 look very promising and many new projects are expected. We want to remain the market share leader and gain an even higher market share. 2021, here we come. For now, stay safe!

What the Pandemic Brought to Me

By Steffen Krohnert, ESPAT Consulting

In the middle of December 2020, Germany went into its second lockdown. It seemed that people were more careless compared to March and April, when COVID-19 pandemic started, and we had to go into the first lockdown. Numbers are much worse now and reaching sad records every day. Too many people did not believe it (COVID-19) was true. The virus exists and is dangerous. They rejected the use of masks and gathered for demonstrations against measures taken by the government and have even been hosting so-called "Corona-Parties".

Lockdown … There seems to be no German word for it, as everyone is using the English word, but it does not change what is behind it. I think the German word "Herunterfahren" fits best – it means shutdown: That is the shutdown of public life, limiting joint activities outside and inside, kindergartens closed, no education in the classroom, completely closing all kinds of entertainment, museums, restaurants, bars, party spots, hotels, vacation areas, theatres, operas, cinemas, concerts, fitness, and swimming centers.

Our beloved German Christmas Markets were cancelled, and New Years' fireworks were not sold, and it was recommended that we not leave the house or gather in any way. The rules are enforced by police controls, and authorities are imposing painful financial penalties … in any case, it's better than getting this painful disease.

All kinds of entertainment closed? Not really — we can take walks and play sports outside. There are a lot of things you can do at home: Refurbish, repair, clean, play games, do puzzles, listen to music, watch Netflix, and who knows,

maybe we will have a baby boom mid of 2021!

But wait, there is more:

We started talking more to our partners, families, and friends; sharing our doubts, concerns, ideas, wishes, and plans on what we want to do differently once this pandemic is over. What will life look like? Will we be back to "normal" quite fast? What will stay, and what will change? Can we take some of the good elements that resulted from the situation into our life after? Some people defined a "new normal" after the first lockdown. Will they define an even "newer normal" after the second one?

I feel sorry for the year 2020. Almost everyone wants to press the reset button and start the year again, delete 2020 from the calendar. People want to forget and are looking forward to 2021. I received Seasons Greetings like I have never seen before. One said "In spite of all adversities, I wish you a Merry Christmas and a hopefully better New Year for all of us."

But what can we learn from 2020, what are the "Takeaways"?

We have a nice German word "Entschleunigung", which means slowing down. It gives us more time to think, to look at the bigger picture, and make decisions wisely. It is the opposite of "Beschleunigung", the acceleration that drives us restlessly through the working day and even after.

Despite all the negative effects, such as people getting sick and dying from COVID-19, losing jobs and fighting for survival, parents that must manage family and job at home all in parallel, kids that can't get the education they need for their bright future, governments needing to take on debt in numbers that we can't even imagine…. there are positive effects too.

First, we see that life continues, whatever happens, and we find a way to deal with the situation. There is always light at the end of the tunnel, and no, it is not the train that is approaching us at high-speed. We need to be optimistic, and follow the rules defined for us by our brightest minds — remember, there is always a team of great scientists and intelligent advisors behind each politician. Second, we see that the world is global and cannot be separated with walls. This is true for climate, economy, people's right to live with dignity, and for viruses too.

I had time to read, study, walk, and hike targeting 10,000 steps a day. I have never discovered my surroundings more and I have never been outside more than in 2020. That alone is a reason why I don't want to delete that year from the calendar. I had time to take care of my house — something I have not done much during the last 8 years when I was "on the road" around 80% of the time travelling worldwide for NANIUM, and later for Amkor Technology before I settled down with my own firm, ESPAT-Consulting, in Dresden, one of the most wonderful places to live and work. I took care of my health more than ever before, started training with a personal trainer twice a week, got a nutrition plan, which I follow — more or less. With restaurants closed, a regular day structure without travels and without heavy business dinners, liters of beer at Oktoberfest, and many cups of mulled wine with a shot at the Christmas Markets, it is definitely easier. You see, you just need to make the best of it.

The Art of Doing Business Virtually

By Keith Felton and Kevin Rinebold, Siemens Digital Industries Software

For us at Mentor, a Siemens business, COVID -19 brought the closure of all our offices and beginning of learning how to work, collaborate, and do business virtually. The interaction with customers and prospects typically happens on a very personal level, with sales and technical account executives traveling to customer locations for meetings, demonstrations, evaluations, seminars etc.

Luckily Siemens was already planning to rollout Microsoft TEAMs, which was accelerated due to the pandemic. For many, it took some time to master and acclimate to the platform, but we were surprised how well customers adapted to the transition to virtual interaction when dealing with their EDA technology supplier. With our field teams no longer flying and/or driving to visit customers, they had more time for quality customer interactions using new multimedia communications tools like TEAMs.

Siemens does not expect that pre-COVID-19 activities will fully resume until a proven vaccine is available, and even then, the amount of travel to meet customer face-to-face will be reduced as doing business using virtual technologies has proven to be, in some cases, more effective, especially from a cost perspective. For us the financial year ended on September 30th and despite the enormous burden and impact of the pandemic turned out to be a year of exceptional bookings and revenue performance.

So, as we look forward to 2021 our first thought and hope is it will bring a vaccine and an end to this deadly pandemic so we can try to get back to some semblance of normal.

On the technology side, 2020 saw a significant surge in companies designing heterogeneous 2.5/3D devices and the discovery that their legacy organic BGA focused design tools were running out of steam.

In 2021, we expect to see more fan-out-wafer-level package (FOWLP) designs turning to panel-based manufacture with companies like DECA Technologies, ASE, NEPES, and PTI leading the charge.

On the performance side of packaging, we expect to see more non-silicon-based interposer like designs emerging as the pressure to reduce costs while increasing device performance and yield increases. All of this will require greater adoption of early and comprehensive prototyping/planning with co-optimization, often referred to as STCO. With more silicon chiplets and substrates being integrated together as a single 3D package, the assembly verification (DRC/LVS) challenge of such designs will grow almost exponentially, driving more change and the need to adopt advanced technologies and methodologies.

While pure silicon scaling has not stopped, the era of huge monolithic CMOS devices being the sole driver of More than Moore is very close to ending being superseded by heterogeneous/homogeneous 2.5/3D IC package.

In summary the era of the dinosaur is ending, long live the era of the mammals……

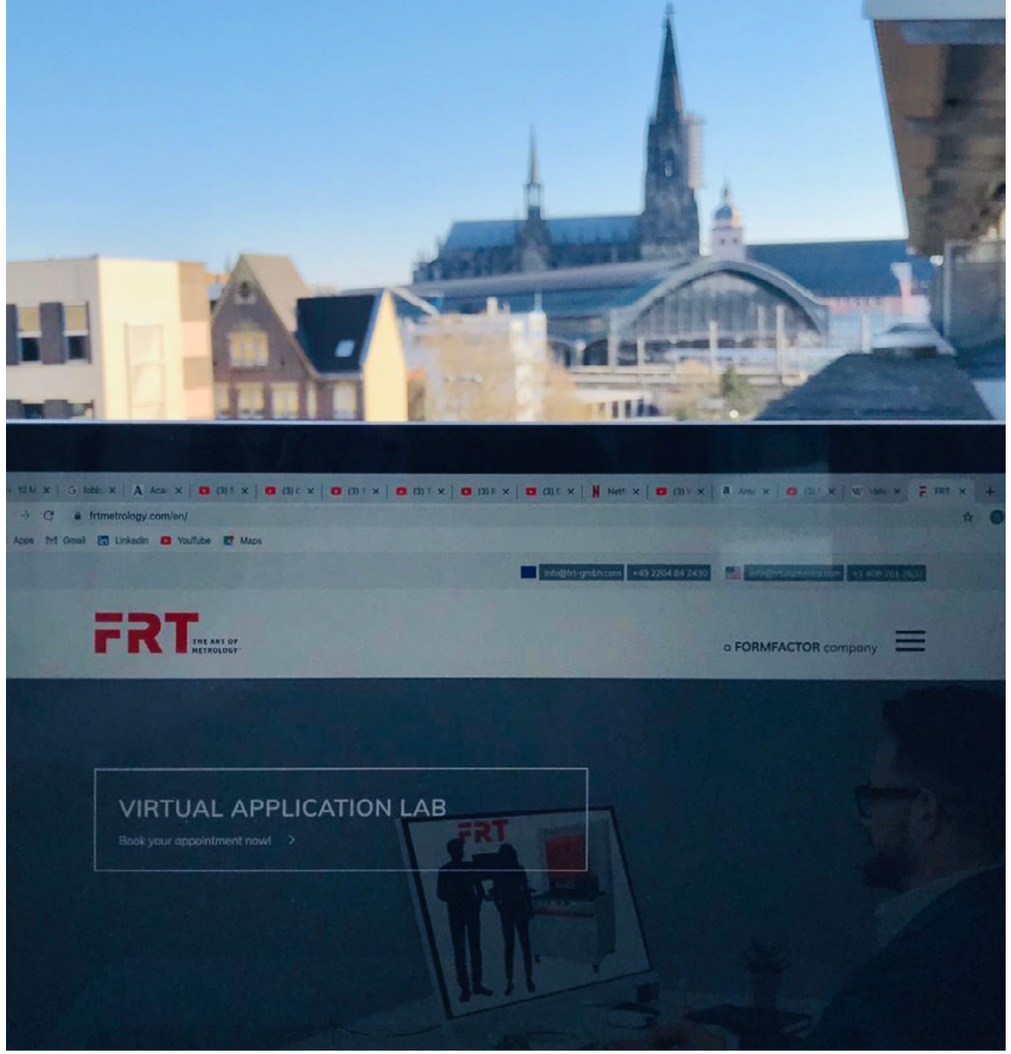
A Start-up Grows Stronger

By Aric Shorey, Mosaic Microsystems

As an early-stage company, Mosaic Microsystems worked hard to navigate the Covid-19 pandemic. Our #1 goal was to keep our employees safe. Fortunately, we had recently closed a $2.25M seed investment from BlueSky Capital and Corning Incorporated, received a Phase II Small Business Innovative Research (SBIR) grant from the National Science Foundation, and a Phase I SBIR award from the Air Force (AFWERX). These helped us to navigate the uncertainties brought on by the constraints caused by the Coronavirus.

We also saw some interesting market dynamics created by the pandemic. Early on, we saw an increase in requests as some companies worked to re-shore some products. Conversely, we saw a number of development activities significantly delayed as our customers had difficulty getting into their cleanrooms to process wafers. Activities that would normally take one to two months were now taking more than six months. There were a few instances where some projects were canceled as customers focused on existing products and often needed to re-align resources to make products with reduced staffing, and/or managing facility shutdowns.

Many of us shifted to working full time from home, but as an essential business, our clean room remained open following all CDC guidelines, and we were able to continue driving the technical



development critical to bringing our products to market. We were able to establish new capabilities, such as introducing 300mm capability to Mosaic's portfolio, and progressed well in our work with the Department of Defense. The funding mentioned above, and customer sales allowed us not only to maintain full staffing levels but also add a key employee.

While the summer months were quiet on the commercial side, we have seen an increase in activity as fall and winter approach and people are beginning to gain confidence with vaccines on the horizon. In the end, Mosaic will emerge from this pandemic stronger than it started.

Setting Systems in Place

By Sarah Trompetter, FRT, A FormFactor Company

During the first lockdown, at FRT, we began sending our employees to their home office within a week — first those with children or special working conditions. As many of our employees worked at desktop computers, new laptops were purchased in short order, and existing ones were retrofitted accordingly.

We introduced a system to reduce contact. The plan was for 50% of each department to alternately work from home, if possible. However, since we actually assemble our tools at our facility, which cannot be done from home, it can sometimes be challenging. Our management team is very responsive to individual needs. So far, we have been fortunate to not have to interrupt production on any day. Measures are adjusted continuously.

In 2021, we hope that the situation will improve. We are most looking forward to being able to visit our customers again or have them come to our facility. We are also looking forward to events and networking! Stay all healthy.

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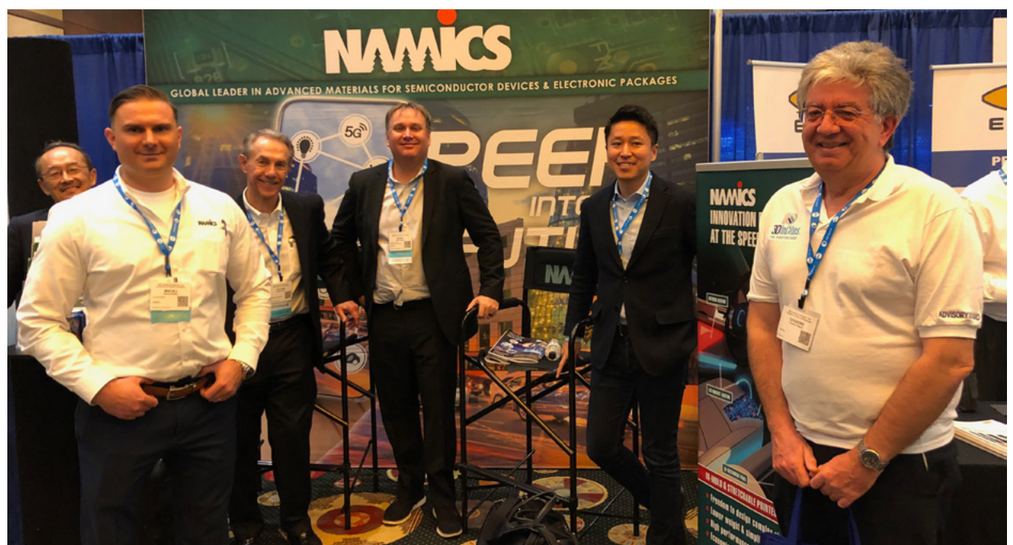
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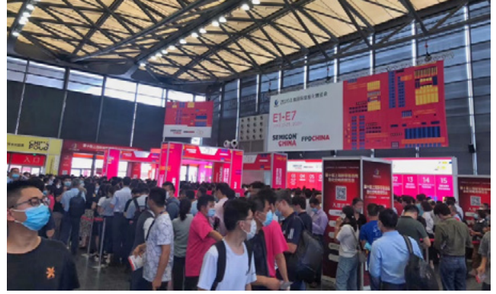
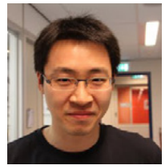


Member photos

Contributing Editors continued from 5

Roland Rettenmeier, co-author of *Fan Out Panel Level Packaging Takes Off* is Senior Product Marketing Manager at Evatec, where he focuses on business development for emerging applications like EMI shielding and advanced IC substrate processing. Rettenmeier is a Mechanical Engineer and completed his executive MBA studies in Austria in 2005. He has experience in electronics and semiconductor manufacturing, managing projects in China, Switzerland, and Austria since 2001.



Jiaqi Tang, Ph.D., co-author of *Artifact-free Decapsulation of 2.5D and 3D Semiconductor,* is the President and CTO of JIACO Instruments, the start-up company he co-founded to commercialize the Microwave Induced Plasma (MIP) machine he developed during while he worked on his Ph.D. degree at Delft Institute of Microsystems and Nanoelectronics (DIMES), Delft University of Technology. His research activities focus on developing a MIP instrument for copper wire bonded semiconductor package decapsulation application.

Ludo Vandenberk, author of *Meeting the Needs of a Demanding Semiconductor Market,* is a senior VP and one of the major shareholders at Trymax. He joined the company in 2005 to develop new semiconductor equipment for the plasma ashing and etching market. Ludo focuses on new business development and is responsible for the worldwide sales and marketing organization. He gained experience in both plasma etching and ashing product performance at Philips Research and Matrix Integrated Systems, respectively.

Kevin Rinebold, co-author of *Adapting to Virtual Communications* is the Technology Manager for Advanced Packaging Solutions at Siemens. He has 30 years of experience in defining, developing, and supporting advanced packaging and system planning solutions for the semiconductor and systems markets. He has defined and pioneered some of the earliest solutions for IC-PKG-PCB co-design. Prior to joining Siemens, Kevin was Product Manager for IC packaging and co-design products at Cadence. He's held similar positions at Sigrity, Synopsys, and Xynetix.

Sarah Trompetter, author of *Setting Systems in Place,* is Marketing Manager for FRT GmbH — a Form Factor company, where she focuses on developing strategies for content marketing and lead management. Sarah studied international marketing and media management, and has advanced experience in social media management, website performance optimization, search engine marketing, content creation, and distribution. Prior to joining FRT, she was the online marketing manager for Yokogawa Deutschland GmbH.

Pascal Vivet, Ph.D., co-author of *Fine-Pitch 3D Stacking Technologies for High-performance Heterogeneous Integration and Chiplet-based Architectures,* is Scientific Director of the Digital Systems and Integrated Circuits Division at CEA-LIST, Grenoble, France. He received his Ph.D. from Grenoble Polytechnical Institute in 2001, designing an asynchronous microprocessor. After four years within STMicroelectronics, he joined CEA-Leti in 2003 in the digital design lab. Pascal's research interests, which span many aspects of circuit and system level design, led him to become project leader on 3D circuit design and integration.

Aric Shorey, Ph.D., author of *Solutions for Glass-based Packaging are Here and A Start-up Grows Stronger,* is the VP of Business Development at Mosaic Microsystems, a company focused on using thin glass substrates in microelectronics and photonics packaging. Eric has been in the precision optics, telecommunications, and semiconductor industries for more than 20 years working on materials processing, characterization, and program management. Before Mosaic, Aric led activities to enable thin glass solutions for microelectronics applications at Corning Incorporated.

Thomas Uhrmann, Ph.D., author of *Die-to-Wafer Bonding Steps Into the Spotlight on a Heterogeneous Integration Stage,* is director of business development at EV Group where he is responsible for overseeing all aspects of the company's worldwide growth. Prior to this role, Uhrmann was business development manager for 3D and advanced packaging as well as compound semiconductors and Si-based power devices at EV Group.

Ralph Zoberbier, co-author of *Fan Out Panel Level Packaging Takes Off* is Head of the Advanced Packaging Business Unit at Evatec. He s more than 20 years' experience in the semiconductor equipment business, with roles in engineering, product management, and global business and sales management. In addition to thin film technology, his technical expertise covers areas including lithography and ECD for both wafer and panel level applications.

The Big Squeeze – Why OSATs Need to Work Smarter continued from 23

environment of semiconductor manufacturing, you will probably not survive. OSATs are not new to data collection and management. After all, testing is part of their name. But test data is product/function focused. In its simplest form it is go/no go. Functional testing may go beyond that, to measure how well it works, if for no other reason than to identify the best devices and sell them for premium prices. Smarter manufacturing requires data on a whole new scale — data that is both deep and broad.

Deep data measures all aspects of the manufacturing process. It measures feature sizes and shapes, but it also measures equipment performance, tracks maintenance operations and consumables, and much more. It provides the basis for correlating differences in product performance with events and variables in the manufacturing process. As processes become more complex, the number of variables quickly exceeds any human's ability to monitor and extract actionable information. Smart manufacturing includes sophisticated analytical techniques, like data mining and artificial intelligence, that can quickly find correlations that would otherwise be invisible. What batch of chemical was that device exposed to? On what tool? When? Was there a tool failure or error condition? Combining product data with tool data yields true process data.

Broad data provides visibility of the lifecycle from end-to-end throughout the entire supply chain, from wafer manufacturing, to device fabrication, packaging and testing, warehousing and distribution, and even into final disposition and use. Clearly, OSATs are only one link in this chain, but they are a critical link. They should ensure their data is captured and structured so that it can be a leveraged in a variety of ways in the future. Whether that be sharing subsets of data to optimize efficiency across the entire value chain or to take advantage of cloud enabled services, OSATs who do this will be more competitive than their conservative counterparts.

The OSAT model needs smart manufacturing

Will history repeat itself? Probably. If you look at the complexity and dimensions of the structures being created by cutting edge advanced packaging processes today, they are remarkably similar to what device manufacturers were doing 30 years ago. Device manufacturers have been through this process evolution and have learned the value of process data. They know that the cost of data pales in comparison to the costs of slower yield ramps, yield-robbing process excursions, and the redirection of human resources to solve problems. They are the competition.

The degree to which OSATs continue as a separate segment is open to question. 30 years ago, there were dozens of major device manufacturers. Today the market has consolidated. There are three or four in the first tier, another half dozen or so in the second tier, and numerous small niche providers. A similar consolidation is likely among OSATs. The question is, will they remain independent or be subsumed by IDMs and foundries. The answer will be determined in large part by the choices OSATs make as they confront the inevitable digital transformation being spurred by Industry 4.0, big data plays, and market consolidation.

In Memory of...

Recently, I received sad news from some of you to let me know about the passing of several industry colleagues. We thought it fitting to pay tribute to them here.

Avi Bar-Cohen, 1946-2020

Avi Bar-Cohen passed away on October 10, 2020. He was an internationally recognized leader in thermal science and technology and was a guiding force in the emergence of thermal packaging as a critical engineering domain. Phil Garrou offers this memory: "I first started working with Avi in the early 1990s when he served as Editor of the IEEE EPS (then called CHMT) journal. In his later life, when he moved to DARPA to become the Director of the ICECool program, he pulled me into DARPA and made me a packaging subject matter expert (SME). We worked on many IEEE and government programs together through the years. In all the years we worked together, I always found Avi to be a hard-working, reliable, and trustworthy individual with a great sense of humor and I will miss his presence in our advanced microelectronics community."

Luke G. England, 1979-2020

Luke England passed away on December 12, 2020, after a hard-fought battle with cancer. His work in the industry included metal research and development for Micron, GlobalFoundries, and Marvell, with multiple U.S. patents to his credit. As 3D expert at GlobalFoundries, he was actively involved in the development of the company's "industry first": a fully qualified chip-package interaction device comprising a 14nm logic die with 5×50µm Cu filled through silicon vias (TSVs), upon which two 14nm test chips that emulate high bandwidth memory (HBM) are stacked. Luke participated regularly as a speaker in industry events including the 3D Systems Summit, IEEE ECTC, and others. I always enjoyed speaking with him.

James R. Drehle, 1943-2020

Jim Drehle passed away on December 29, 2020. An electrical engineer, he worked for Hewlett Packard/Agilent Technologies for 36 years, retiring in 2005. He's best known to us for his involvement in the International Microelectronics Assembly and Packaging Society (IMAPS), where he served as President on two different occasions 1997 and 2006 and was a member of the board of directors for years. He was an avid fisherman and most weekends you could find him in his boat on a lake enjoying his favorite pastime.

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