3DInCites™ EST. 2009

YEARBOOK

COVER STORY:
Looking ahead to inspire the innovators of the future

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STAFF

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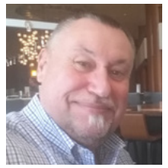

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Joe Montano, the author of *Protecting Devices During a Supply Chain Shortage*, joined the Delphon team in late 2020 as President and was recently appointed to the position of President and CEO effective January 1, 2022. He has spent his entire 25+ year career in electronics and electronic materials technology segments, with experience spanning from the R&D bench to Sr. VP positions and now President and CEO. Before joining Delphon, Joe was the Global Business Director for MacDermid Enthone's Advanced Electronics division before moving to Sr. VP of Sales and Marketing for Intermolecular Inc. There, he helped orchestrate the acquisition of Intermolecular by Merck KGaA, Darmstadt, Germany in 2019.

Ajay Sattu, the author of *Vehicle Electrification Driving Supply Chain Evolution* joined Amkor in 2018 and is Director, Automotive Product Marketing at Amkor Technology, Inc. He is focused on automotive electrification, ADAS, and infotainment product marketing and strategy. Before joining Amkor, he worked for Infineon, managing the technology and product development of wide-bandgap semiconductors. Ajay has published more than ten articles and presented at several conferences in the emerging technologies area of GaN and SiC.

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John Volz, the author of *The Foundation is Set: Ready for Growth in 2022*, is Senior Vice President Business Development - Office of the President, Reno Sub-Systems. An industry veteran with 35 years of semiconductor capital equipment experience, John comes to Reno from Ferrotec's Temescal division, where he was Business Development Director. Before that, John held leadership roles at SSEC LLC, Genus, Inc., Matrix Integrated Systems, Inc., Mattson Technology, Inc.; and various management positions at Silicon Valley Group, Inc. and Plasma and Materials Technologies, Inc.

Dr. Thomas Uhrmann, the author of *Another Strong Year Ahead for Hybrid Bonding Thanks to Heterogeneous Integration*, is director of business development at EV Group where he is responsible for overseeing all aspects of the company's worldwide business development. Before this role, Uhrmann was the business development manager for 3D and advanced packaging as well as compound semiconductors and Si-based power devices at EV Group. He holds an engineering degree in mechatronics from the University of Applied Sciences in Regensburg and a Ph.D. in semiconductor physics from the Vienna University of Technology (TU Wien).

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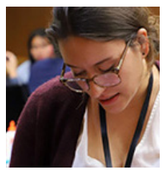
Devan Medeiros, the author of *How My Internship at Mosaic Helped Me Grow*, is a chemical engineering student at Rochester Institute of Technology. He recently completed an 8-month internship at Mosaic Microsystems.

Matan Utschen is a Mechanical Engineering student at Arizona State University. He spent his internship at EV Group's North American HQ in Tempe Arizona.



Louise Greco, the author of *From Macro to Micro: Learning Microelectronics Firsthand at StratEdge*, is an Engineering Tech at StratEdge & Aerospace Engineering student at Southwestern College.

Bhaumi Panchal, the author of *Why An Internship in Fan-out Technology Was My Dream Come True*, graduated from the University of Passau with a Master's degree in Mobile and Embedded Systems. She is currently working for ERS electronic as a Fan-out Product Engineer.

Dolores Termini is currently a graduate student at the New Jersey Institute of Technology studying material science. Dolores earned her undergraduate Engineering degree with a focus on optics and lasers. She is currently an Applications Lab Intern at Veeco based in Somerset, New Jersey.

Keeping Up with the Times

By Françoise von Trapp

I'm sitting here, flipping through memories of 2021 like it was a Rolodex, sorting through the highlights, lowlights, and Aha! moments to share with you in this Yearbook editorial. And then I realize I'm dating myself, because how many people under the age of 35 know what a Rolodex is? But an analogy to Hubspot or some other CRM — that's customer relationship management, for you old-timers — doesn't give the same mental picture so I'm sticking with it.

Why do I care if someone under the age of 35 understands my reference? Because believe it or not, one of my Aha! moments of 2021 was discovering, by the power of Google Analytics, that the largest segment of our readers (42%) falls between the ages of 18 and 34. And almost 38% falls between the ages of 35-54. In fact, only 20% of our readership is older than 55.

This is a pretty big deal. Because as more of the semiconductor industry workforce approaches retirement age, the talent shortage is worsening. It's more important than ever to reach a young audience – one that might consider a future in microelectronics and semiconductor manufacturing if they knew how interesting and exciting it is.

That's one reason we started the **3D InCites Podcast** – to meet our audience through a medium that they use often. Who listens to podcasts? According to Edison Research's Infinite Dial Report, 49% of monthly U.S. podcast listeners are aged between 18-34, 40% between 35 and 54 years old, and 22% are aged over 55. Just look at how those numbers line up with ours!

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ARE YOU LISTENING?

We've also dedicated this Yearbook issue to inspiring young engineers to pursue careers in the semiconductor industry. In our Cover Story, *Looking Ahead to Inspire the Innovators of the Future* (**Page 20**), I speak with Lena Nicolaides, Sr. VP, and GM at KLA, about the company's efforts in recruiting, retaining, and sustaining talent. KLA's initiatives extend from within the company itself, to the surrounding communities, reaching children as early as kindergarten age. Additionally, we invited interns at our member companies to submit essays on their internship experience, in the hope of inspiring others to join this exciting industry. Their stories begin on **page 30**.

Getting back to in-person events was a major highlight of 2021. Steffen Kröhnert represented 3D InCites at SEMI Europe's Packaging Technology Seminar and SEMICON Europa. I attended both the IMAPS International Symposium and SEMICON West and brought our podcast recording equipment along to capture all the conversations we've been missing over the past two years. You'll find photos beginning on **page 46**.

Both SEMI and IMAPS recognize the importance of reaching a younger audience. We're working with these industry organizations to help spread the word about the importance of sustainable semiconductor manufacturing and diversity equity and inclusion (DEI). We partnered with SEMI to be the Official Podcast of SEMICON West 2021, and plan to expand that relationship in 2022.

One of our first big moments of 2022 is becoming Official Industry Partners with the International Microelectronics Society (IMAPS). We've always had media trades, but as we recognize the synergies between our two organizations, we decided to formalize the relationship.

Our first order of business is to integrate the 3D InCites Awards and DEI fundraising more definitively into the IMAPS Device Packaging Conference agenda. Beth Keser, president of IMAPS, served as one of the technology judges and will help present the awards. Our Mural Fundraiser is happening again, and we're also hosting the first-ever Hike for DEI, sponsored by KLA. 100% of the proceeds from the mural and hike benefit the 3D InCites DEI Fund, established in 2021 to help tech start-ups owned by women and underrepresented minorities grow and thrive.

It goes without saying that the lowlight of 2021 was the emergence of the Omicron variant. Just when it looked like things were getting back to normal, there it was to remind us that COVID is something that we're going to be dealing with for some time to come. But don't let it get you down. Despite it, our industry is on an upward trajectory and we've all had a pretty good year. Remember that, and try to stay safe, everybody!

Françoise

Looking at the Global Semiconductor Expansion Through Polarized Lenses

By Dean Freeman, FTMA

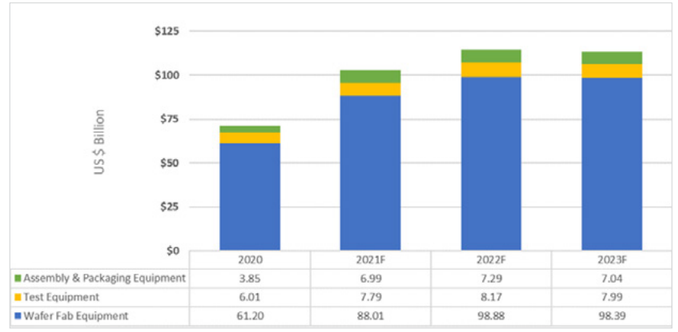
The song, *Happiness is Lubbock Texas in My Review Mirror*, has a special meaning for me, as due to a Texas ice storm, a day trip to Lubbock, TX was extended. Thanks to a determined Southwest Airlines team, a group of us managed to get home only a day later, as opposed to potentially spending the weekend in Lubbock in the snow and ice.

As the semiconductor industry moves into 2022, I can't help but wonder if any executives are thinking: "Happiness is 2021 in the review mirror". Perhaps they have mixed feelings about a year riddled with ice storms in the southwest of the United States that shut semiconductor plants down, as well as droughts in Taiwan, a factory fire in Japan, shipping and supply chain issues for material, equipment, and semiconductor manufacturers, a hybrid work environment increasing manufacturing challenges, and a talent shortage. This has all contributed to the widely highlighted chip shortage. That, paired with unprecedented demand due to what could be called a paradigm shift in the electronics industry due to electric vehicles (EV), 5G, smart everything, and edge computing, is making things interesting, to say the least.

However, even with all the challenges, this has been a banner year for the microelectronics industry. From a chip perspective, the Semiconductor Industry Association (SIAs) fall forecast has the industry ending 2021 at 25.6% growth. This equates to $553 billion in growth for 2021, the strongest growth year since 2010. From an equipment and materials perspective 2021, according to a recent press release by SEMI, total equipment is expected to reach a historical high of $103 billion, 44% year over year growth, with WFE reaching 88 billion, and the assembly and packaging sector just shy of $7 billion, and test at $8 billion.

IC Insights estimates that total Capex will reach $152 billion; also a historical high. The market research firm says these strong growth rates have been driven mostly by logic and analog expansion. The top four equipment companies— Applied Materials (AMAT), ASML, Lam Research, and TEL — all look like they will top the $10 billion mark for equipment sales, and ASML looks like it has close to a 12-month backlog going into 2022 (Figure 1).

As the industry moves into 2022, most CEOs seem to be cautiously optimistic on their quarterly calls, but as this industry has learned over time, the outlook can change



	2020	2021F	2022F	2023F
Assembly & Packaging Equipment	3.85	6.99	7.29	7.04
Test Equipment	6.01	7.79	8.17	7.99
Wafer Fab Equipment	61.20	88.01	98.88	98.39

Figure 1: SEMI 2021 Year-end total equipment forecast by segment. (Source: SEMI)

in the blink of an eye. The last time I remember ASML having a 12-month backlog, the outlook changed very quickly as I'll discuss below.

What Will 2022 Bring?

What does this mean for 2022? At first look; good news. In its **December press release**, the SIA is forecasting an 8.8% growth in semiconductors. **IC Insights** is predicting 11% growth. So, from a chip perspective, the growth will continue. This is being driven, in part, by the extended chip shortage.

Many articles written on the shortage have the tightness or shortages extending through at least the first half of 2022 and possibly longer. However, this pertains mostly to logic and particularly automotive, due to the increasing demand for electronics in automobiles. The SIA forecast shows fairly even revenue growth across all sectors for 2022, perhaps suggesting that supply and demand will come further into balance in 2022, and the shortage will start to dissipate (Figure 2).

On the Equipment Side

From an equipment perspective, SEMI is predicting 11% growth in 2022 after a staggering 44% growth in 2021. The 11% for equipment growth for 2022 seems to be close to the consensus from the earnings calls from the "Big Four" equipment companies. In 2023, SEMI is predicting a very slight downturn.

This is where it gets a bit interesting. Ajit Manocha, President, and CEO of SEMI presented the following at SEMICON West: Between 2020 and 2024 a significant number of fabs will be built. Twenty-five 200mm fabs and 60 300mm fabs. This accounts for 18% capacity growth for 200mm and 48% growth for 300mm in the 2020–2024-time frame. For 200 mm 14 of those 25 fabs are in China, two in Taiwan, and three in Japan. For the 300mm fabs, 15 are in China and 15 are in Taiwan. Six are targeted for the United States, and Europe and Israel are seeing a significant increase in activity as 10 are targeted for Europe and the Middle East. This suggests the potential for strong growth for the foreseeable future. Especially since it appears that China will continue to build no matter what the environment.

Another positive out of this fab forecast is that there is little to no inventory for 8-inch used equipment. This means that unless that 200mm fabs have a source for 200mm equipment, they will be buying new equipment, which will then have a significant impact on margins due to paying off that newer equipment. I suspect this might slow the start-up of some 200mm fabs, but also be extremely beneficial to 200mm equipment suppliers.

So, What Could Go Wrong?

Chip demand is currently extremely strong. Consumers in the United States are fueling electronics demand. The automotive industry needs to catch up and build inventory. 5G is rolling out, as is WiFi6, and industry is digitizing which strengthens demand for cloud computing, and artificial intelligence (AI).

What can slow the industry down?

There are the usual suspects. Covid 19, a talent shortage, trade issues. To me, these are minor bumps in the road and, except for the trade issue, can be resolved with some creative thinking, such as training programs, which used to exist when I entered the industry. My concerns are something bigger on the horizon.

The first is what instigated the last major downturn in the industry. In 2008 and 2009 wafer fab equipment (WFE) declined 32% and 46% respectively due to the Lehman Brothers financial crisis. Going into SEMICON West 2008, equipment backlogs were 6-12 months, the future looked very bright. and then three months later the industry was scrambling. According to the **Chip History website**, analysts were not aware of the impending crisis. Some analysts were concerned, but the hot electronics market and the huge WFE backlogs made it difficult to send a message of doom and gloom.

So, what does the Lehman crisis have to do with today's market? While in the western world the financial markets are in pretty good shape. In China, multiple bankruptcies are in progress. Evergrande real estate, and **The Tsinghua Unigroup**, parent of YMCT, are both struggling financially and are working to restructure.

While the total debt of both companies is well under 500 billion, there are some thoughts that this could cause a significant financial crisis in China. If **Evergrande fails** and does not get bailed out, it is likely there will be a slowing of investment in new projects. If YMCT goes under, there would probably be a limited impact on the NAND business, but there could be a shock wave for the equipment industry, as there could be a pullback on those 29 new fabs scheduled to start-up in the next two years. It is a challenging situation to predict. Beijing may help to avoid any crisis, but it is also possible Beijing will let the companies fail. It happened in the LED industry when it was overbuilt in China a while back, so it could also happen in this situation. Currently, it is a wait-and-see situation.

The US/China trade issues also cloud the future of the equipment outlook. From my perspective, the US Government trying to stop China's chip and electronics expansion are a bit like trying to put the toothpaste back in the tube, since previous administrations encouraged electronics growth in China.

There is always the outside chance the commerce department will prohibit the sales of US semiconductor equipment to any fab in China, and pressure U.S. allies to follow suit. In the near term this would make the semiconductor shortage even worse, and in the long term have the potential of US or European companies reshoring parts of that chip business. However, this transition would take at a minimum, 4-6 years, and it would need significant government financing, significantly more than the current, hopefully-by-the-time-you-read-this-passed, CHIPS act is proposing.

> *"Happiness is 2021 in the review mirror. HAPPINESS IS A FULLY LOADED FAB"*

In the short term, it would reduce the semiconductor equipment sales by approximately 25% until that chip business was relocated. It would also potentially create the opportunity for the Chinese equipment makers to up their game and develop competitive products for the Chinese market.

The other upcoming challenge for the industry is the inevitable oversupply of chips that will be created by all of these new fabs. Economics has driven the chip industry. Economics has driven the fabless model and made TSMC the success it is today. I don't remember the source, and I probably have written it in these blogs before, but "Happiness is a fully loaded Fab". The oversupply probably won't happen in 2022, but maybe that's why SEMI has a flat forecast predicted for 2023.

So, while at the moment, the future of the semiconductor chip, packaging, and equipment industry looks very bright, I'm making sure I'm wearing my polarized lenses so I can hopefully see the contrasts as they come down the road.

Fall 2021	Amounts in US$M			Year on Year Growth in %		
	2020	2021	2022	2020	2021	2022
Americas	95,366	**118,835**	**131,084**	21.3	24.6	10.3
Europe	37,520	**47,126**	**50,467**	-5.8	25.6	7.1
Japan	36,471	**43,581**	**47,621**	1.3	19.5	9.3
Asia Pacific	271,032	**343,419**	**372,317**	5.1	26.7	8.4
Total World - $M	440,389	**552,961**	**601,490**	6.8	25.6	8.8
Discrete Semiconductors	23,804	**30,100**	**32,280**	-0.3	26.4	7.2
Optoelectronics	40,397	**43,229**	**45,990**	-2.8	7.0	6.4
Sensors	14,962	**18,791**	**20,913**	10.7	25.6	11.3
Integrated Circuits	361,226	**460,841**	**502,307**	8.4	27.6	9.0
Analog	55,658	72,842	79,249	3.2	30.9	8.8
Micro	69,678	79,102	83,980	4.9	13.5	6.2
Logic	118,408	150,736	167,396	11.1	27.3	11.1
Memory	117,482	158,161	171,682	10.4	34.6	8.5
Total Products - $M	440,389	**552,961**	**601,490**	6.8	25.6	8.8

Figure 2: World Semiconductor Trade Statistics (WSTS) Forecast Summary (Source: WSTS) Note: *Numbers in the table are rounded to whillions of dollars, which may cause totals by region and totals by product group to differ slightly.*

IFTLE 500: We've Come a Long Way, Baby!

By Phil Garrou, 3D InCites

Insights from the Leading Edge (IFTLE) believe it or not, has reached #500! I hope this message reaches all of you free of COVID and ready to move on in this exciting period for Advanced Microelectronic Packaging. For those of you that have not been on board for the full trip, let me share a little background history.

Background 2004-2010

After retiring early in 2004 following a 27-year career at Dow Chemical, I started writing Advanced Packaging articles for Pete Singer and his leading microelectronics magazine, "Semiconductor International" (SI). While SI's focus was on front-end chip fabrication, there was readership interest in the leading packaging technologies of the day.

Post-2000 wafer-level packaging (WLP) was just beginning to catch on as Pete Elenius and Flip Chip Technology (FCT) began licensing its bumping and WLP technology to all the major packaging houses in Taiwan and Korea. WLP was of special interest to me since, while at Dow, my electronics business had helped FCT develop its "Ultra CSP" WLP and low-cost bumping technologies with our Benzocyclobutene resin (BCB) (Figure 1).

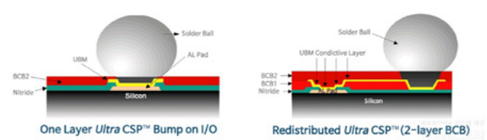


Figure 1: Versions of FCT's Ultra CSP WLP.

In 2005, Kenny Williams at the Microelectronics Center of NC, hired me part-time to help with its new DARPA 3DIC program and I quickly became convinced that vertical integration was the next big thing. I knew from the beginning that this technology would take substantial time to catch on, but little did I know how long it would take. My 2005 article, "Future IC's Go Vertical", was one of the earliest magazine articles of the 3D IC genre and one of the most highly referenced at the time.

My early SI articles included:

- October 2000 - "Wafer Level Packaging Has Arrived"
- Oct 2004 - "The Wafer Level Packaging Evolution"
- Feb 200 - "Future ICs Go Vertical"
- October 2006 - "Wafer-Level 3D Integration Moving Forward"
- Dec 2006 - "Opto- WLPs for CMOS Image Sensors"
- April 2007 - "Posturing and Positioning in 3D ICs"
- Oct 2008 - "3D ICs Coming Together"
- Nov 2008 - "3D ICs Enter Commercialization" (Figure 2)

Figure 2: Phil was a regular contributor to SI and penned many articles on hot packaging topics.

In 2006, I rose to the rank of "Editorial Advisor". By the summer of 2007, it had become obvious that SI was shrinking in page count due to fewer and fewer print advertisers, and that internet publications had become the wave of the future. At that point, Pete asked me to think about a weekly blog to keep the world updated on what was going on in Advanced Packaging.

On July 28, 2007 "Perspectives From the Leading Edge" (PFTLE) was born with the first blog being a little personal bio and a promise ……"For all the latest in advanced packaging stay linked to PFTLE……."

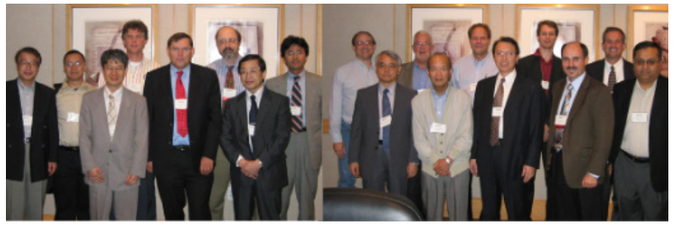


Figure 3: Back row: Xie (Penn State), van Doremalen (Philips), Garrou, (Microelectronic Consultants of NC), Tanaka (U. Tokyo), Patti (Tezzaron), Shaper (U. Arkansas), Enquist (Ziptronix), Morrow (Intel), Keast (MIT LL), Front row: Motoyoshi (Zycube) Aoyagi (AIST), Beyne (imec), Koyanagi (Tohoku U) Yamada (IBM Japan), Kada (ASET), Lu (RPI), Franzon (NC STATE), Patel (Altera).

Over the next few years, I developed my irreverent reporting "style", which included a blend of hard-hitting technical content mixed with sarcasm and tongue-in-cheek humor in articles such as :

Going Vertical in Whitefish - 09/09/2007

What's the Capital of NY State? - 10/14/2007

A Rose by any Other Name is NOT 3DIC Integration - 11/20/2007

3D Integration: Evolution or Revolution? - 03/16/2008

If It's Thursday this must be San Jose - 06/08/2008

It All Depends on What the Meaning of 'it' Is - 09/17/2008

Mechanical Bulls, Rollercoasters, and CIS with TSV - 09/26/2008

Ziptronix Opens the Kimono - 10/14/2008

Like Mick Jagger said: You Can't Always Get What You Want – 11/24/2008

Fisk, Buckner, and Pasta in the North End - 12/31/2008

Like Swallows Returning to San Juan Capistrano - 03/20/2009

Ginkgo Biloba - 09/12/2009

Having been editor of my high school newspaper years before (Brooklyn Technical HS class of '66), I knew all about clever headlines and having roots in the bowels of Hell's Kitchen, NYC, it was impossible for me not to be sarcastic and/or tongue in cheek when I wrote.

Figure 4: Phil's Four Horsemen of 3D IC integration – cost, test, thermal management, and design.

By the time we published PFTLE 100 in 2009, we were covering the presentations at the first global conference focused on 3DIC sponsored by the IEEE CPMT Society (now the IEEE EPS (Electronics Packaging Society) and chaired by Paul Franzon and me. Figure 3 captures the organizing committee, a veritable who's who for 3DIC in 2009.

A few months later PFTLE, introduced the Four Horsemen of 3DIC Integration": Cost… Test… Thermal Management…Design, to emphasize that more was needed than the basic process flow before commercial 3D stacking could be introduced into the mainstream market (Figure 4).

In early 2010, with much of the 3D unit operation processing work behind us, PFTLE began to focus on efforts of standardization, which most agreed had to start with memory stacks.

Then, after 128 weekly blogs, in April of 2010, Reed Elsevier, the owners of SI sold off its magazine portfolio and pulled the plug on Semi International. As the SI web pages were shut down so were the links to all my work! Lesson for all current and future bloggers …Internet blogs are not archival!

IFTLE Begins – 2010

Pete Singer quickly moved over to PennWell publishers and the newly merged (2009) Advanced Packaging / Solid State Technology franchise and brought me with him. There were worries concerning the copyright on "PFTLE", so I reluctantly changed the title to "Insights from the Leading Edge (IFTLE)" and thus it has remained ever since. In June of 2010 we were back online as IFTLE with the following statement:

As Jack Nicholson said in the Stephen King classic "The Shining" …I'm baaack…!

That first IFTLE covered updates from the 2010 Electronic Component Technology Conference (ECTC), and an announcement that the IEEE had bought out the EIA and now had full ownership of the ECTC conference. I was especially proud of that last item since I had been working on accomplishing that acquisition for several years during my IEEE Electronic Packaging Society (EPS) [at that time known as CPMT] presidency and that of Bill Chen who followed me.

The relationship with PennWell's Advanced Packaging/ SST franchises worked well for nearly 8 years and 395 IFTLE blogs, but I could see trouble was brewing once again towards the end of this period when contributors' checks were being delayed for many months at a time. There was always some excuse, but the inevitable closure finally came.

Phil Garrou and Françoise von Trapp celebrate during the 2018 3D InCites Awards.

This time I acted quickly and talked to my old friend, Françoise von Trapp who had established the 3DInCites community back in 2009. Seemed like a good spot to re-establish IFTLE and she was quick to welcome me on board. This time I kept the IFTLE acronym and we started up with number 396 with an update on the **DARPA CHIPS program**, which had started in 2017, and of which I was a participant. This of course was the precursor to today's chiplet mania in the advanced packaging community (Figure 5).

Things at 3D InCites for the **100+ blogs** have gone as smooth as silk. Thanks to **FRT (now Formfactor)** who sponsored IFTLE for 2 years, and to our current sponsor, **EV Group.**

Looking back, there have been several things that I have intentionally tried to do with IFTLE.

The number one premise for this blog has always been to share with our worldwide readership what was being presented at the major and minor conferences held around the world on topics pertaining to Advanced Packaging. There are very few of us who have the budget or time to allow us to personally attend all these meetings, so PFTLE/IFTLE thought we could try to share what went on and get that information back to our readership.

But, instead of covering these meetings the way traditional reporters would with inconsequential comments from authors or titles and a one-line summary, IFTLE selected key presentations and shared the key slides from those presentations. Did I always pick out the most important papers? Who knows…but you certainly got an in-depth look at what I picked out.

Although the front-end IC techies had treated the back-end packaging techies like serfs for the past 50 years, IFTLE tried to make it clear that the packaging community needed to stay up-to-date on what was going on in the front end, or we would be like blind people trying to paint portraits. In that vein, considerable time has been spent looking at what the front end was doing and the impact that could have on the back end.

Similarly, though I am not a design or test expert, I thought it was important to stay on top of the major design and test activities especially as we were trying to bring 3D ICs to commercialization.

From my 25+ years at Dow experience, which ranged from R&D through new product commercialization, I knew how long it took to get new concepts through the pipeline. Thus, while the commercial marketing houses like Yole Développement were out there proposing rapid market acceptance of advanced packaging like 3D TSV stacking technology, IFTLE was always throwing cold water on such inflated market numbers and short adoption time frames, which in hindsight has been very accurate.

My experience indicated that a proven concept in R&D usually takes at least a decade to reach its first $1MM in sales. Again, in hindsight, 3D IC has taken even longer than that to gain commercial acceptance because of the enormous changes that were required in the infrastructure and business supply chain.

New things take time to really be understood and adopted, so when IFTLE found a technology that it thought could have a significant impact, we intentionally covered it multiple times to update and for reinforcement. My best example of this would be Ziptronix and its direct bond interconnect (DBI) process.

Ziptronix spun out of Research Triangle Institute in 2001 without a primary application or a customer base. It took the Ziptronix team a while to realize that their oxide bonding process had relevance to CMOS image sensors (CIS), but once they did, the industry quickly adopted the technology and ran with it. While Toshiba was the first to adopt it in late 2008, licensee Sony has built their leading CIS market share on these oxide-oxide and copper-copper bonding technologies.

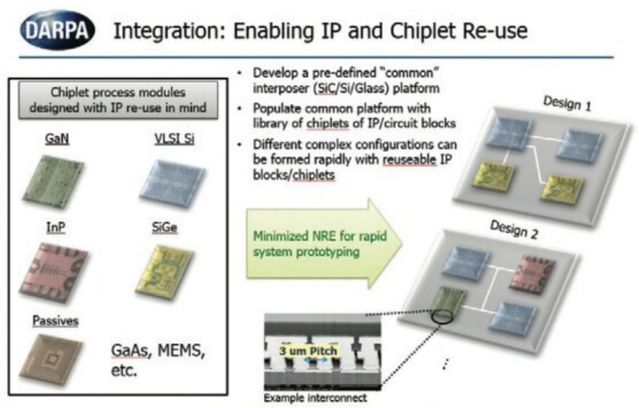


Figure 5: Phil kicked off his tenure at 3D InCites with a post about the DARPA CHIPS Program.

IFTLE has probably covered this technology 10 times or more over the decade. Our interest proved correct as we have recently seen all the major players (TSMC, Intel Samsung, etc.) having what we now call "hybrid bonding" on their roadmaps to replace copper pillar bumps as we moved to ever-finer interconnect features. Was the commercial community waiting for the original Ziptronix patents to expire or was this simply a technology ahead of its time? I'll let you answer that.

Another technology that IFTLE has highlighted more than a dozen times is micro-transfer printing (MTP). It came out of a college laboratory in Illinois around 2005 as the start-up, Semprius. It is basically a massively parallel pick and place technology looking for an application. I worked with Semprius and its CEO Joe Carr (a long-time Dow colleague) in its early days but left when they decided to focus on manufacturing solar panels (IFTLE is NOT a fan of expensive energy sources).

While their solar efforts didn't succeed, the technology persisted and eventually spun out again as X-display, under Chris Bower, a company using the technology to move massive quantities of tiny LED components to fabricate LED displays. It has also become clear that MTP is also relevant to heterogeneous integration and, with the help of X-Fab, lives on as X-Celeprint. While MTP has not yet been included on the roadmaps of Intel, Samsung or TSMC just yet, my gut tells me there is something there and it will find larger applicability… eventually.

So what do I think have been some of the technical highlights that IFTLE has covered in the last decade?

General Observations:

- #1 is watching packaging evolve from an afterthought to the important position that it now holds in the overall industry.
- IFTLE has enjoyed watching long-time colleague Rao Tummala and his GaTech packaging center brethren bring microelectronic packaging into the educational mainstream.
- IFTLE has watched ASE's Bill Chen pour his heart and soul into the Heterogeneous Integration Roadmap. That kind of commitment is rare and should be applauded.
- IFTLE loved watching Peter Ramm and Mitsumasa Koyanagi **get the credit they deserved** for being pioneers in the development of 3DIC integration.
- IFTLE has watched Eric Beyne from his early days as a grad student to his status as a worldwide leader in advanced packaging.
- IFTLE is thankful for having had the opportunity to have worked with advanced packaging colleagues like Jack Balde, George Messner, Avi Bar Cohen, Iwona Turlik, George Harman, Ted Tessier, Pete Elenius, Herb Reichl, Jan Vardaman, Paul Franzon, CP Wong,

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Adaptive Control: The “Holy Grail” in Semiconductor Smart Manufacturing

By Dongkai Shangguan, Ph.D., Adaptix

Artificial intelligence and machine learning (AI/ML) can have various applications in smart manufacturing for semiconductor fab, advanced packaging, and electronics manufacturing, and it typically involves several key elements: sensing, connectivity, predicting, and control. As recognized by many industry organizations, smart manufacturing matures through several levels: reactive, preventive, predictive, and autonomous (Figure 1).

Adaptive control is the “holy grail” in AI/ML for semiconductor smart manufacturing. There are various AI/ML platforms in the industry that can be used for supply chain management, new product introduction (NPI), production planning, traceability, all the way to predictive maintenance, productivity improvement, process, and yield improvement, etc. The latest AI/ML platform can take you right to the highest level, with sensing, connectivity, predicting, and control all-in-one while providing a scalable, open, and cost-effective platform that seamlessly and progressively integrates all the key elements (Figure 2).

The AI/ML platform can utilize data from existing sensors within the machine, often without the need for additional sensors. The edge-first solution can integrate into other cloud and edge-based services, allowing legacy system data connectivity to nearly all major automation vendor components and providing flexible data management tools to move OT data securely and reliably across complex enterprise edge-to-cloud network architectures. The ML models offer the capabilities for predictive optimization – for machine process, and its control intelligence capability can work directly with the machine, once approved by the customer, for adaptive control of the machine itself. As such, the AI/ML platform not only offers capabilities for observability and monitoring, but also further offers great capabilities for predictive analytics, optimization, and control (Figure 3).

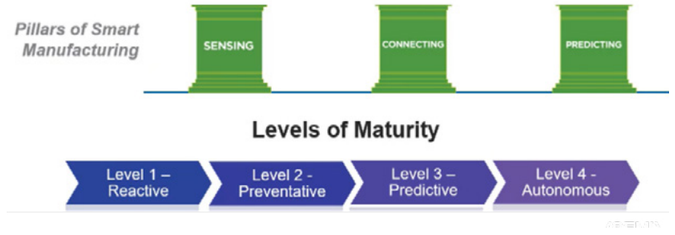

Figure 1: Pillars and maturity levels of Smart Manufacturing (Source: SEMI).

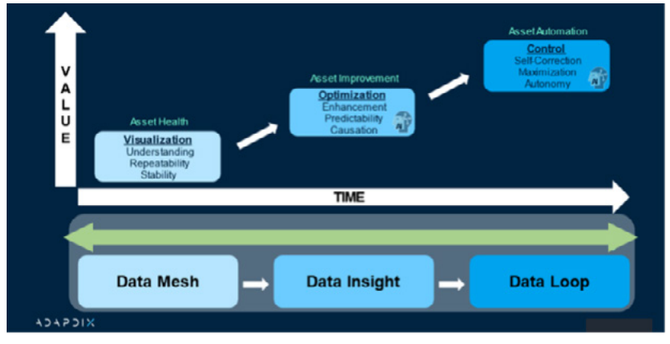

Figure 2: Modules in AI/ML platform for different levels of applications (example).

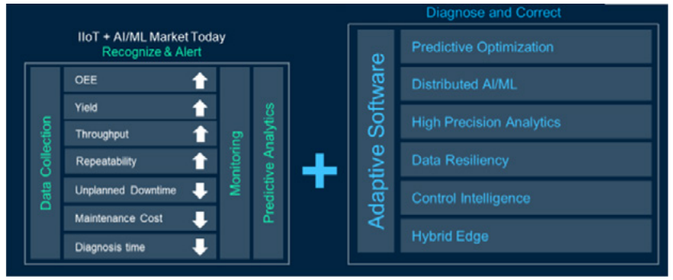

Figure 3 Applications of AI/ML for electronics manufacturing (examples).

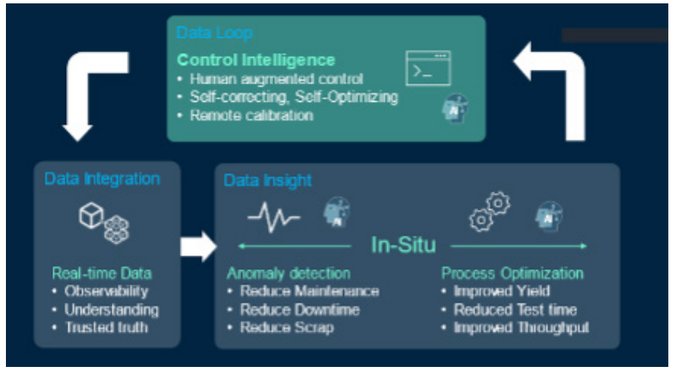

Fig. 4 Architecture of an AI/ML platform (example).

Architecture

As an example, the software solution combines advanced AI/ML with a distributed, edge-based architecture (Figure 4). The platform connects and ingests multiple edge data streams (e.g., process logs, machine data, and instrumentation data in a time-synchronized fashion) in real-time – within millisecond cycle time. It can also collect full-stack data from the customer's end-to-end operations and perform real-time synchronization and validation of critical system data.

The flexible and containerized architecture can support a variety of protocols at the edge (including proprietary brownfield protocol deployments), thus allowing the platform to easily integrate with industrial equipment for data ingestion. The open and scalable architecture built specifically for the distributed edge environment can help avoid the overhead of moving all data to the cloud or centralization location from the get-go. The open and extensible architecture allows

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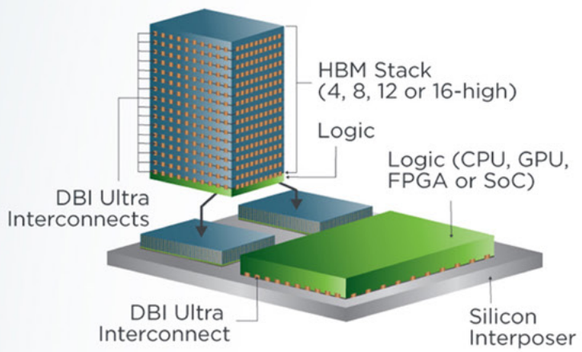
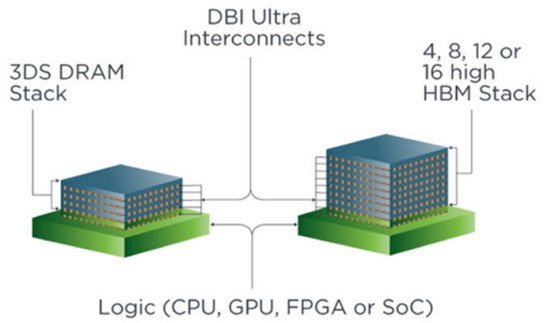


3D Integration



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Looking Ahead

to Inspire the Innovators of the Future

A Conversation with KLA's Lena Nicolaides

By Françoise von Trapp

2021 was a big year for the semiconductor industry, and 2022 is expected to be even bigger. Ironically, despite the mayhem it caused, the chip shortage and its impact on the global supply chain turned out to be the best advertising we could have hoped for in our industry. While those of us who work in the semiconductor industry once lived in relative obscurity, the whole world now knows how important semiconductors are to our everyday lives.

Semiconductor manufacturers all over the world are gearing up to meet demand by building new fabs and adding capacity to existing ones. The downstream effect is impacting global equipment and materials suppliers, as they too expand facilities and open new ones to ensure a well-oiled supply chain. The entire semiconductor ecosystem is in a hiring frenzy to support all this activity.

Well before the pandemic, industry seers predicted a strain on the semiconductor workforce as more engineers and technologists approach retirement age. At the same time, many of those just entering the workforce with degrees in science, technology, engineering, and math (STEM) are being drawn to what appears to be hipper, sexier STEM-related career paths. They dream of being part of the metaverse: Facebook. Google. Amazon. They want to design cool apps, pursue careers in biotech, or renewable energy. How can we interest them in something as "boring" as manufacturing tools or materials that make semiconductor devices? They didn't realize how cool it was to be part of the ecosystem that makes all these things possible. Until now.

Innovating a Talent Pipeline

Where many people see challenges, Lena Nicolaides, Sr. VP and GM at KLA, sees opportunity (Figure 1). She is passionate about the semiconductor industry and the magic it makes happen. Early on in her role at KLA, Nicolaides spearheaded multiple efforts to promote STEM education. "We need innovators for the future," she says. She's made it her focus – leveraging her role at KLA – to inspire the next generation to not only pursue degrees in STEM but to parlay those degrees into careers in the semiconductor industry.

"Semiconductor CapEx is increasing at greater than 40% year-over-year growth. But without the talent nothing happens," she said. "We need innovators, and a lot of them, for the future of the industry."

As a company, KLA has always put a focus on talent, but now they are doubling down their efforts as the situation becomes even more critical. But it's not enough to recruit new talent. How do you sustain it? How do you retain it? Nicolaides firmly believes the talent journey begins as early as elementary school.

"As we innovate for our tools, we innovate with our people," she says. "These are the people who create our systems. Starting the education process in elementary schools allows us to build a talent pipeline for innovators of the future."

She says it's exciting to go into classrooms and explain how KLA is one of the companies that enable the acceleration of chip production to address the current shortage. Because it impacts consumers' ability to purchase everyday goods like new cars and appliances, young children now understand how important computer chips are.

"Making semiconductor technology relevant to the home has given us a fantastic opportunity. We need to leverage that so that we can attract talent. When parents talk about how they can't buy a car because of the chip shortage, it makes kids understand the importance of chips and want to work in the industry. We need to convey they can work on cool things like artificial intelligence (AI), and state-of-the-art optics and imaging technology. We need to show them how the industry can positively impact the environment by reducing energy use."

Figure 1: Lena Nicolaides and Stephen Hiebert, Senior Director of Marketing for KLA's LSA-SWIFT division, are passionate about the role KLA plays in innovation.

The Great Resignation

In the aftermath of the pandemic, the US experienced what has been dubbed “The Great Resignation” as women and men of all professions took stock of their lives and made decisions about their careers that lead to record numbers of people leaving their jobs.

Nicolaides says that at KLA, and across the semiconductor industry, demand has increased. Part of that is because the industry is thriving and was also able to pivot to a virtual work environment.

“People have moved companies, some have taken early retirement, but overall, there is an increased curiosity about the industry,” she said. “The pandemic has taught us all to retain our talent and flexibility is key.”

For KLA, that meant working from home, working when you can, and showing up to a Zoom meeting with a child on your lap. "Flexibility and empathy empower the organization and make for happy engineers," she said.

Nicolaides also thinks that the pandemic equalized things. Zoom conferences on individual video screens, versus a conference call with a room full of people, brought people closer together and made it possible to build relationships with colleagues in other regions. "It created a sense of equality in the way we do business and brought our divisions together," she said.

The semiconductor industry is testing a hybrid model blending work from home with work at the office allowing flexibility. As companies emerge from the pandemic, the work environment will further morph and evolve.

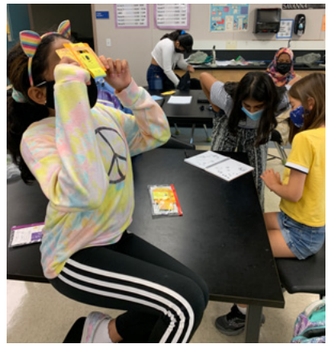

Figure 2: These 2µm resolution paper microscopes give students an idea of how tiny semiconductors can be, and the role electron microscopes play in the manufacturing process.

Nicolaides is especially proud of KLA’s STEM Inspectors program that kicked off in 2019, in partnership with Santa Clara Unified School, Santa Clara, Calif, to bring STEM into the classroom (Figure 2). Using a hands-on approach with 2µm paper microscopes, students acquire useful STEM skills while learning how electron microscopes are used in the semiconductor industry. The pilot was so successful, it was launched globally, and already 1000 students have participated in it.

The breadth of career paths that a degree in engineering can open up is not readily apparent or rarely discussed. That's why, as part of the STEM Inspectors curriculum, students are introduced to the education paths and many career opportunities available in the semiconductor industry.

KLA supports multiple education programs and many of its employees invest their time to support and expand these programs. Examples include:

- **Science is Elementary** – KLA employees volunteer monthly to teach science modules to kindergarten students at Alexander Rose Elementary School in Milpitas.
- **First Robotics** – KLA Foundation sponsors over 20 high school robotics teams that compete in the annual FIRST Robotics Competition. Students learn how to design and build robots while developing critical collaboration skills.
- **SEMI High Tech U** – As a Global Partner, KLA Foundation supports HTU efforts in helping students understand education and career pathways that lead to high-tech fields.

One Person at a Time

Nicolaides remembers when KLA first hosted a module of SEMI HTU and how satisfying it was to see the sparks of interest light up. This outreach program offers three-day experiences to high-school students who are interested in pursuing careers in STEM. The students participate in hands-on workshops and group challenges to learn about STEM-related fields. They visit manufacturing facilities, learn how to write a resume, and participate in mock interviews.

Madhav Nekkar, a freshman at Westmount High School, was so inspired by what he learned, he wrote a personal letter to Nicolaides expressing his gratitude to KLA for hosting the event in 2013. He went into detail describing the experience, and how it planted a seed to pursue a degree in STEM. She had his letter framed and it hangs on the wall in her office as a reminder that if you can reach just one person, the effort is worth it (Figure 3). Madhav graduated with a STEM degree and is now working in the industry.

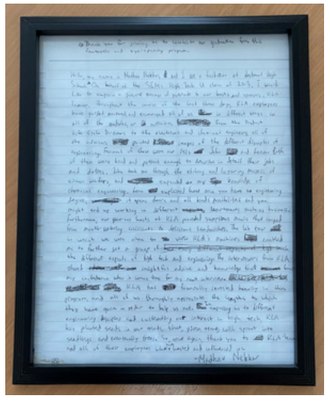

Figure 3: Nicolaides proudly displays this thank-you letter from SEMI High Tech U graduate, Madhav Nekkar, to remind her that even reaching one person makes the efforts worthwhile.

The Gender Gap

Even with industry-wide initiatives underway, gender inequality continues to plague the semiconductor industry. According to a global survey of engineering students and career engineers, women tend to seek a career path in engineering later than men. A higher percentage of male engineers set out to become engineers while still in high school, while women decide as undergrads (Figure 4).

Again, Nicolaides believes the problem can be traced back to elementary-age children, who are generally given conventional gender-defined toys. Puzzles, train sets, and Legos are listed under "Boy's Toys", while dolls, toy kitchens, and Easy-Bake Ovens are listed as "Girls Toys”.

For its part, KLA works to create opportunities and increase long-term access to educational resources to support girls and under-represented communities throughout their unique journeys, including STEM fields. By supporting Taiwan Girls Camp, Habitat for Humanity, and Alliance 4 Girls, KLA provides resources for young girls and women to overcome the challenges of gender inequality.

Helping the gender gap at all levels within KLA, Nicolaides is the executive sponsor for the Women in STEM Empowered (WISE) employee resource group (ERG) that works to attract, advance, and provide more opportunities for women at KLA. WISE helps KLA’s employees grow and navigate their development path at KLA.

A Career Born out of Curiosity

"The curious mind will gravitate towards STEM," says Nicolaides.

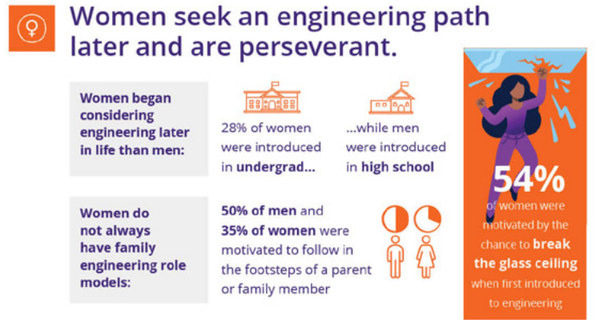

Figure 4: Data show that women seek an engineering path later and are perseverant.

According to **KLA’s Engineering Inspiration Report**, engineers today are inspired by purpose and technology: Things like the digital era, sustainability, and social and societal issues (Figure 5)

Nicolaides often draws on her 20-year career in the industry, and specifically at KLA, to illustrate the wonder of the semiconductor industry. She says she’s never bored and continues to be inspired to innovate.

“Building these tools – inspectors that find these small, tiny things – it’s so fulfilling to see a tool go into production,” she says. “As engineers, we all have in common the desire to see our ideas come to fruition.”

She thinks many people underestimate how big engineering is and how many fields there are. People can start as engineers and go on to have a very diverse career path. For example, Nicolaides began as a research scientist and is now a general manager.

With a foundation in STEM, the semiconductor world is your oyster – from R&D, processes and technology, to operations, sales, support, and beyond. Do you want to travel the world? Work in cutting-edge technology? Move to marketing? Be a writer? Climb the corporate ladder? The semiconductor industry has it all.

“There is a role for every personality within our semiconductor industry,” says Nicolaides. “From engineers to marketing, to technicians, application engineers, human resources, corporate roles… tell me your degree, and there’s probably a job you can have.”

Sustaining and Retaining Talent

"How do we strengthen our talent? We enable them to grow from within," says Nicolaides. “Retention starts from Day One.” She identified three keys to retention.

Open Communication

“Employees want to feel like they are part of something bigger," notes Nicolaides. If they fully understand the mission and goals of their division and the outcome of their work, they have context and are more likely to stay with the company. Alternatively, companies who silo their employees to protect their IP,

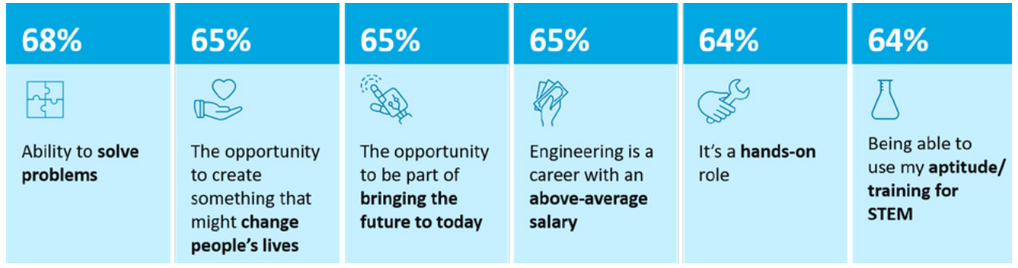

Figure 5: When first introduced to engineering, around two-thirds of engineers and students were highly motivated by the ability to solve problems, the chance to change people’s lives, and the opportunity to bring the future to today.

tend to see less commitment. And during the pandemic, more frequent communication was needed to enhance transparency and strengthen the team connections.

Ongoing Development

“It’s important to be at a company that develops you,” says Nicolaides.

At KLA, this means professional development, continuing education, and ERGs. For example, the WISE ERG holds regular events.

One recent panel discussion focused on how to navigate your development path at KLA. One employee talked about first working on the development of one inspector system, and then followed that with a role in the applications division, leveraging the knowledge gained during tool development. Another employee described their journey from engineering into a marketing role.

They also have an in-house learning center where new hires follow a standard curriculum and have access to a wide range of training courses as part of their KLA career path. Employees can take advantage of other enrichment programs and pursue master’s degrees.

Show Appreciation

The third element on the continuum of retention is to show appreciation. KLA regularly celebrates employee achievements. It’s the little things that go a long way. Appreciation is shown, with several award programs, at both individual and team levels. The pandemic further demonstrated the need for appreciation and connecting with team achievements.

"It's about understanding the talent you have, and empowering the talent you have," said Nicolaides. “That is how you inspire others to follow this path.”

Conclusion

From kindergarten to a career at KLA, inspiring the innovators of the future is a lengthy and complex journey. But industry leaders like Nicolaides understand that it’s worth every step. The key to success is to keep looking ahead.

The new Plus Building at the KLA Milpitas campus has room to host large employee meetings, a modern café with rooftop patio and ample space for employee collaboration.

On-site coffee shop at the KLA campus in Milpitas

Convertible walls can open and let the California sunshine into the new multi-purpose space at the KLA headquarters.

Considerations in Power Amplifier Package Design

By Casey Krawiec, StratEdge

Understanding the role of compromises and trade-offs in the design process

Electronic packages serve many purposes including protecting, connecting and cooling a device. If any of these are done improperly, the chip is rendered inefficient at best or useless altogether. For that reason, the design, construction, properties, and capabilities of the package selected are critical to ensure optimal device performance.

Temperature is one of the main factors that affect performance. High-frequency devices can suffer a loss of efficiency as temperatures at the chip level increase. Every degree of heat that can be dissipated adds to the efficiency of the device as well as to its useful life.

The package plays a significant role in thermal management. Proper thermal management is essential for high frequency and high-power semiconductor devices such as gallium arsenide (GaAs) and gallium nitride (GaN). In particular, GaN-on-SiC devices have incredibly high power densities and the design of the electronic package can dramatically affect their performance.

Several types of engineers are typically involved in the electronic package design cycle. Mechanical engineers, materials engineers, electrical engineers, and thermal engineers contribute most often, but sometimes manufacturing or industrial engineers might also be included. So, the compromises and trade-offs begin at the engineering level but don't end there. People from the accounting, quality, purchasing, assembly, and sales and marketing departments may also have input.

Within this assortment of people that have such different levels of education, experience, and expectations, it can be difficult to please everyone. The person in charge of the final package design, more often than not, feels pulled in a lot of different directions. But if everyone understands that many issues beyond their own must be considered, the team can achieve a workable design that meets the customer's major objectives.

Package Layers

Thermal considerations address two areas, thermal expansion, and thermal conductivity. A useful tool in considering electronic package designs is to consider the package as a series of stacked layers. Working with and thinking about packages in terms of layers can simplify thermal dissipation and expansion analysis. Viewing packages as layers is a useful way to understand 3D interactions in the package structure. This is the basis for thermal simulation modeling.

The leaded power amplifier (LPA) package is an example of layered construction. It begins with a combination base and heat sink, topped by an alumina insulating layer, a metal lead frame, and a lid. (Figure 1.)

The surface mount power (SMK) package is very similar to the LPA package but has vias to carry the signal from the top conductor pads to the bottom of the package. The leads on the bottom of the ceramic are coplanar with the bottom of the base. With the leads trimmed short, this package is appropriate for surface mounting (Figure 2.)

The LPA and SMK package examples are ideally suited to many power amplifier applications. They use a single heat sink layer of copper composite or copper laminate that has a high thermal conductivity and is also well matched to the temperature coefficient of expansion of most devices. It's also convenient that they are designed to operate over a broad range of frequencies. LPA packages have excellent performance from DC to 23 GHz and have bolt holes for securing the package to the printed circuit board (PCB) and chassis. SMK packages operate from DC to 26 GHz and have the convenience of being surface mounted, which simplifies the PCB design.

Conclusion

Many factors need to be considered when designing the optimum power amplifier package, including thermal dissipation and expansion requirements. Usually, no single consideration can dominate, so the design decisions end up as compromises. One simple method to aid understanding of the issues in assembly and function of the package is to view the package as layers. This simple analysis is useful to understand both the CTE and heat flow. Simulation tools can be used to analyze the impacts of expansion mismatch and thermal conductivity on the reliability and performance of the final assemblies. These tools can be used to estimate if material choices are practical and to what degree a material or design change will impact a performance parameter of the package.

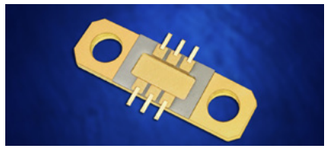

Figure 1. LPA Package.

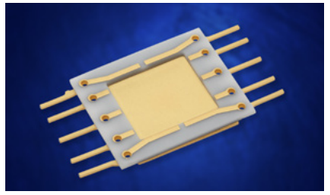

Figure 2. SMK Package.

Vehicle Electrification Driving Supply Chain Evolution

Dr. Ajay Sattu, Amkor Technology, Inc.

If the recently concluded CES® 2022 is any indication, the automotive industry is yet again in the crosshairs of both consumers and industry experts alike. Whether it's the new electric vehicle (EV) model introductions, color-changing technologies, or concept cars, automotive companies are slowly transforming themselves from manufacturers to technology platform providers. Vehicle electrification is one of those megatrends that has now morphed from a novel trend to accepted reality. Several environmental, economic, and social factors are influencing vehicle designs and the new powertrain choices. However, some of these choices and corresponding component design and manufacturing aspects may lead to a supply chain evolution in the coming years.

Market Trends

CO2 emission mandates set by various regulatory agencies are driving electromobility growth. For example, as shown in Figure 1, the chart on the left shows normalized CO2 emissions for each of the four major automotive markets, while the chart on the right shows how CO2 emissions can be reduced by various degrees of electrification. The internal combustion engine (ICE) has nearly 100% carbon emissions. In contrast, mild hybrid electric vehicles (MHEV) use a small motor to aid the ICE, providing a 15% emissions reduction. A battery electric vehicle (BEV or EV) uses only a DC battery and motor and thus produces no carbon emissions. Through various powertrain architectures and proliferation, within the next five years, nearly 25% of all vehicles produced will be electrified with the number increasing to around 50% by the end of 2030[1]. This huge growth is due to increases in expected demand, reductions in the cost of the DC battery, and anticipated growth in the charging infrastructure.

Figure 1: CO2 emission standards and vehicle electrification[4].

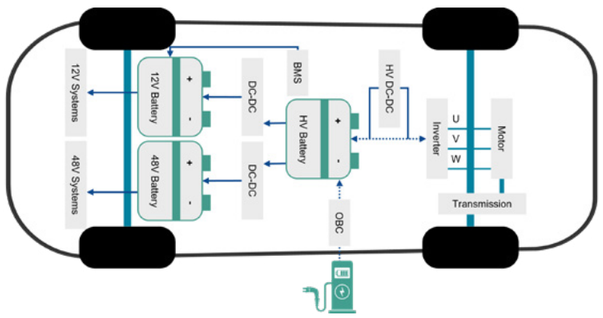

Figure 2: Simplified schematic of an EV powertrain.

As a result, power semiconductors used in EV powertrain systems will see huge growth. To better understand this growth, let's examine a simplified schematic of an EV powertrain (Figure 2). The critical blocks that enable the main functionalities are the onboard charger (OBC), DC/DC converters, and the main inverter. The critical components that enable each of these circuits are power devices, used as switching elements. At the system level, a key priority for EV designers is maximizing the efficiency of all these circuits to enable a better range between each battery charge. As the system requirements increase, so do the requirements on the cost ($/kW) and power density (kW/l) of the power electronics. Currently, cost targets are roughly 5 $/kW, whereas power density is around 12 kW/l. These targets are expected to reach 3 $/kW and 60 kW/l by 2035[2]. To achieve these goals, semiconductor suppliers need to offer superior solutions including newer power technologies such as silicon carbide (SiC) and gallium nitride (GaN) devices, and use cost-efficient power module packages.

Power Module Packaging

In main inverter applications, power modules must address performance and reliability targets within thermal, electrical, and mechanical constraints. While the bulk of the electrical performance is addressed by the semiconductor devices, power module packaging plays a vital role in meeting the thermal and mechanical targets. However, electrical performance can also be improved by reducing parasitic resistances (R) and stray inductances (Ls) of the package. Ls is especially important to reduce overshoot voltages during switching; Ls of a power module results from the substrate metal parts, wire bonds, and lead frame/bus bars. One of the ways to minimize these losses is to reduce the current loop geometrical length and area. Wire-bond-free concepts such as double-sided soldering and sintering on ceramic substrates are better solutions to lower Ls. One such solution, a double-sided cooling (DSC) molded module, is shown in Figure 3a, where wire bonds are replaced with sintering for the current path between collector and emitter of the insulated gate bipolar transistor (IGBT) switch. The DSC module structure not only reduces the electrical parasitics but also offers enhanced thermal efficiency by removing heat from the top and bottom sides of the package through the substrates.

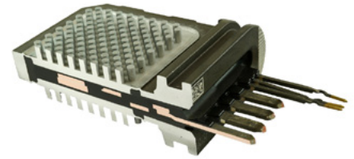

Figure 3a: Double-sided cooling molded module cross section. Figure 3b: Power module with pin-fins for direct cooling [5].

Power cycling and higher ambient temperatures subject power modules to large temperature excursions. So, a cooling system that does not complicate system design and increase cost becomes increasingly important. One way to address these concerns is power module designs with pin-fins (Figure 3b) that share the cooling system used by the motor or engine. For extended reliability, heat must be dissipated effectively, which can only be achieved using low thermal resistance materials. Higher thermal conductivity ceramics such as aluminum nitride (AlN), silicon nitride (Si3N4), and copper (Cu) with a direct cooling structure can be used to reduce the overall thermal resistance. Whether it is a baseplate-free solution such as a DSC module or a pin-fin power module, the packaging industry needs to consider several technologies for next-generation power modules. These include interconnection advancements such as thick gauge (>5 mil) Cu wire, Cu clips, advanced substrates such as Si3N4 with active metal brazing (AMB), die-attach and substrate attach using silver (Ag) or Cu sintering, Cu or AlSiC baseplates, and silicone gel or epoxy resin encapsulation.

Supply Chain Evolution

The power module packaging market has long been fragmented and dynamic. To understand the appeal of this segment, let's look at the module cost breakdown as shown in Figure 4a. Manufacturing and raw materials are nearly 55% of the total module cost[3]; in a power discrete package, these same elements are generally < 20% of the total cost. Historically, power module manufacturers have supplied relatively low-volume and high-price market segments such as industrial, rail, and renewable energy. Given the impending growth of the power module market due to vehicle electrification (Figure 4b)[3], the module supply chain may see several changes. For example, non-automotive suppliers with power module expertise can either choose to expand into the automotive market by themselves or by partnering and licensing technology with traditional automotive suppliers.

In situations where traditionally closed geographical ecosystems existed, some suppliers have started to diversify their business or regional portfolio. The geographical expansion has increased to take advantage of packaging technologies such as substrates, die-attach, and encapsulation.

The automotive industry has long been a high-volume, low-price arena. With the growth in the power module market, competition will increase and suffer from price pressures leading to partnerships to reduce costs and simplify market entry. On the positive side, module technology is well understood, and suppliers have known to release products with excellent performance and reliability. For non-power module makers such as outsourced semiconductor assembly and test (OSAT) suppliers, entering the power module market presents an appealing case since they can easily leverage their current expertise in ramping products to high volume with proven reliability and an appealing cost structure. One final factor that is favorable for OSATs is automakers increasing willingness to venture deep into the supply chain for the inverter module design to differentiate themselves from competitors and to control costs.

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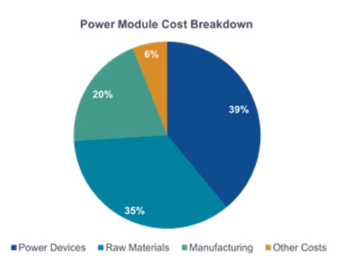


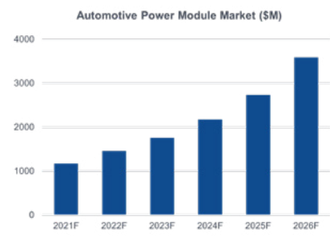


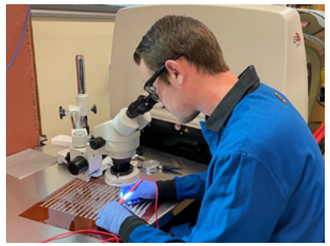
Figure 4a: Power module cost breakdown[3]. Figure 4b: Automotive power module market (in $M)[3].

Through The Eyes of Our Interns

The semiconductor industry is experiencing a massive talent shortage as veteran engineers start plotting their retirements, and students in science, technology, engineering, and math (STEM) programs are either unaware of the opportunities awaiting them in the semiconductor industry, or just have a wealth of other STEM-related careers to choose from. Many of our community members are addressing this by creating robust internship programs that allow students to "try before they buy". Last summer, we invited our member interns to share their experiences through essays. We were going to choose the best, but they were all so good and varied, that we decided to feature them all here. Participating companies included Brewer Science, ERS, EV Group, Mosaic, StratEdge, and Veeco.

What it's Like to Intern at a Top Workplace Award Winner

By Matt Bowie, Brewer Science



Matt Bowie performs electrical test on printed electronic components.

This past summer (2021) was one of the most interesting and educational summers of my life. I finished my junior year studying electrical engineering at Missouri University of Science and Technology when I received an email about an internship opportunity at **Brewer Science**. Brewer Science is an international company based in Rolla, MO. They are known for their research and manufacturing of materials used in the semiconductors, microelectronics, and smart devices industries.

The position was for a Printed Electronics Intern based in Springfield, MO, where I attend most of my classes. Soon after I applied and interviewed, I was offered the position. I could not have been happier! I knew the kind of work that Brewer Science is involved with, and I was excited to be a part of it!

As a printed electronics intern, I have the privilege of working alongside scientists and engineers who develop processes to print electronic circuits and sensors onto flexible substrates. It is very interesting to see everything that can be done with printed electronics and all the challenges that come along with it. It is also interesting to see the entire process of developing a device. Everything from initial design to manufacturing and final application is done under this roof and being a part of it is very exciting!

The best part of being an intern at Brewer Science is that I am treated more like an engineer than a traditional intern. I am part of the engineering meeting, where we discuss the issues we may be having and how best to solve them. During these meetings, my voice and input are heard, not pushed aside as worthless ideas of a student. The feedback I receive during the meetings and the results I observe while carrying out the decisions helps me learn more about physics and chemistry and help me develop a better problem-solving mindset.

I knew a little bit about Brewer Science before starting my internship, but I had no idea how innovative and supportive the company culture was until I started. We are all encouraged to learn more about our industry and the company. Brewer Science has a "Walk a Mile" Program that allows employees to shadow other employees to learn more about the different areas and projects of the company.

We are also encouraged to have "10% Projects," where we take 10% of our time to research a topic of our interest or work on a small project that we are interested in. One of my favorite things is how information is not heavily compartmentalized. I have never asked a question about a project and been told that it was none of my business. I think that this coupled with the Employee Stock Ownership Program is the reason Brewer Science has been **awarded a Top Workplace** award nine times.

I have learned a lot since I started last summer. I learned about research and development in the semiconductors industry. I also learned about what I value in a company. I know now that I want to work somewhere with similar company culture as Brewer Science after graduation. I would recommend that any college student consider interning at Brewer Science. Interning here has taught me so much and has shown me what I want to look for in a workplace.

Why an Internship in Fan-out Technology was My Dream Come True

By Bhaumi Panchal, ERS

Bhaumi Panchal gained experience on wafer and panel debonding and warpage adjustment machines.

I joined ERS electronic GmbH as an intern in fan-out (FO) technology from October 2020 to June 2021 as a mandatory part of my master's degree in Mobile and Embedded Systems at the University of Passau. My internship at ERS gave me great exposure to the inner workings of the semiconductor industry and allowed me to work on some very interesting projects.

During my internship, I was a part of the R&D team in the FO department that develops ERS's wafer and panel debonding and warpage adjustment machines.

My father owns a mechanical workshop, so I grew up watching him work on different machines, which inspired me to want to do the same. I remember being so fascinated by the mechanics and wanting to understand how everything worked. Getting hands-on experience with the complex machines and thermal chucks of ERS was, therefore, a dream come true for me.

With training, support, and guidelines from my colleagues, I was assigned the task of testing and monitoring the ADM330, an automatic thermal debonding machine for 300 mm wafers. This was my first real work experience, so there were many things I was unfamiliar with and had to quickly learn to do. For example, I didn't have much experience in documentation and troubleshooting, but with the help of my colleagues, I learned to get a handle on it.

In parallel, I also got the chance to help on a software project, which was intended for the equipment tests. During my master's program, I had gained some experience coding with Python, but this project required me to learn how to code with C#, which I hadn't used before. Again, this was a challenge for me, but my colleagues supported and placed their confidence in me, which motivated me to take it on.

I enjoyed this project because I got to solve real-world problems instead of the more theoretical projects I had at university. As I gradually improved, I got a real sense of achievement, which boosted my confidence and ultimately allowed me to add a valuable skill to my list of competencies.

During this internship, I learned many things about the semiconductor industry, and I still find it incredible to think that the machines I have been working on are being used by companies all over the world and are contributing to the production of devices that you use in your everyday life.

I also valued the employee events, like Friday meetings and occasional get-togethers, which brought together everyone from the company and the big intern community consisting of other students with whom I could share my experience. I always found myself surrounded by colleagues who were ready to support me, motivate me, and push me in the right direction. Most importantly, the internship has been a great introduction to the industry for a semiconductor novice and machine enthusiast like me, and I am grateful that my career path started with an organization like ERS electronic GmbH.

From Cubes to Chips: One Engineering Student's Journey

By Maten Utschen, EV Group

Maten Utschen's interest in engineering began with an obsession with Rubik's Cube.

It all started with a Rubik's Cube…

When I was in middle school, I liked to struggle with new concepts and would look for ways to challenge myself. It was during this time that I found what became my ongoing project (and some might say obsession), the Rubik's Cube. I spent an entire night teaching myself to solve the original 3x3x3 Rubik's Cube, and my fate was sealed. The 3x3x3 lead to the slightly larger 4x4x4 Cube, and then to the 5x5x5, all the way to the 7x7x7 Cube, with 218 moving pieces to solve.

In 7th grade, when I let a classmate play around with the cube, a piece came loose, causing the entire mechanism to fall apart. That weekend, I spent hours putting it back together, and I was shocked about how difficult it was. I watched YouTube videos, asked my parents for help, visited various forum pages – you name it – until I finally figured out how to reassemble it. Once that last piece smoothly went in, my sense of satisfaction was through the roof! I felt so accomplished being able to create a moving mechanism from what seemed like a bunch of random shapes, and I think that this was truly the first step on my journey into mechanical engineering.

As a freshman in high school, I was introduced to 3D modeling software: Autodesk Inventor. I wasn't satisfied learning how to create different shapes and simple dimensioning; I knew I could do more, and I dove into learning the software on my own. For my final project in that class, I created a fully functioning model of the original 3x3x3 Rubik's Cube in Inventor. This was a great challenge for me because I learned a ton about the mechanism of a Rubik's Cube and how it works together to function. In an engineering class at a local community college during my high school senior year, I recreated the Rubik's Cube model again in SOLIDWORKS, another 3D printing software. Creating the model in the program wasn't enough, however; I wanted to print a functioning 3D prototype. I researched the mechanisms inside the high-end Rubik's Cube brands to create the best possible Rubik's Cube that I could. After struggling with a couple of different ideas, I designed and manufactured one of the smoothest Rubik's Cubes that I still own today.

By this point, I knew I wanted to study engineering in college, but I still had to choose a discipline within the field: I loved learning about mechanics, but I was also fascinated by chemistry. This led to a lot of thought and debate as I tried to settle on a specialty. In the end, I chose mechanical engineering, because it's broader, and I knew that it would introduce me to many more fields in engineering. After making that decision, I chose **Arizona State University**, because its strong mechanical and chemical engineering program would allow me to focus on mechanical engineering and provide me with a backup plan if I wanted to change to chemical engineering.

And EVG has brought me to MEMS (and more) …

Junior year at ASU is the time to investigate internships that will help students pick a career path to enter after graduation. I wanted to look for something that had major mechanical engineering concepts, but also included chemical engineering. My research led me into the semiconductor industry. The industry's critical placement in today's world, as demonstrated recently by the well-publicized chip shortage and growth of 5G, the Internet of Things, and the rise of Smart Cities, showed me that the semiconductor industry would have both the job security and the life-long opportunities for growth and problem-solving. This industry combines both my passions: a strong side of looking at the mechanics of all the expensive and large machines, as well as chemicals and chemical reactions. I was convinced that I wanted to have an internship in the semiconductor industry.

EV Group (EVG) was the first company I came across in my research. I talked to a couple of different people from EVG at various career fairs, learning that a previous intern was also a mechanical engineering student like me, and I began to feel that EVG was the place for me. Additionally, EVG appeared to be both progressive and inclusive in its business culture, especially within the STEM community.

By maintaining a calm work environment and the reassurance that we are a **family**, EVG is consistently ensuring that everyone feels that they belong and are valued and supported. Another thing that impressed me at EVG is the near balance between male and female engineers in the technology department. It is humbling to see a real effort to include women in STEM, rather than it being such a male-heavy industry. All that won me over towards EVG, and it's why I decided to apply for the internship here.

My time at EVG has been challenging, fun, and eye-opening. I look forward to coming to work and learning everything there is to know about the semiconductor industry. My days are spent in the cleanroom, working hands-on and side-by-side with EVG process engineers. I've been part of the team, solving complex puzzles in real-world customer applications, learning about the chemistry in the cleanroom, and about how all these big and technical machines work. I've been shadowing processes for actual customers, as well as running test samples of my own, making me feel that I am truly contributing to the team at EVG.

My co-workers are kind, fun, and everyone is always helping each other out. One of the goals for my internship was to experience the industry, in a real way, and EVG has delivered on that and more. I can confidently say that my experience at EVG has been the perfect application of my education at ASU. I have taken what I have learned in my undergrad and applied it to the major concepts in my internship. It's changed how I view the engineering field and I love that I have found a new passion that is certainly not going away anytime soon.

A Classic 80s toy, the Rubik's Cube, fueled my passions of struggling with new concepts, wanting to challenge myself, figuring out how things work, and designing better, more mechanically functional objects. Now, I'm about to graduate from Arizona State University as a Mechanical Engineer, and I'm excited to see where my adventure with EVG will take me.

How My Internship at Mosaic Helped Me Grow

By Devan Mederios, Mosaic

My name is Devan Mederios, and I recently had an eight-month-long internship at **Mosaic Microsystems**. I had an incredible experience working with this organization and have learned so much.

I am a chemical engineering major at **RIT**, and at Mosaic, I was able to able to apply a lot of the knowledge I had learned from school. Personally, learning on the job is much more enjoyable to me than learning in a classroom, and Shelby Nelson and David Levy both took me under their wing and allowed me to learn and grow as an engineer. I am very grateful to them for trusting me and allowing me to play such a significant role in the company.

One of the first things Shelby explained to me when I started was that I am here for a reason, and that was to help Mosaic grow. Knowing I was an integral part of the organization drove me to be the best every day.

The work environment at Mosaic was one of a kind. Being a small company, I had the chance to connect to each employee. This was important to me because it leads to better communication, better teamwork, and an overall better experience.

Kyle Liddle was one of the employees with whom I formed a great relationship. He and I had great communication in the lab, leading to high efficiency when it came to getting the product out the door and to the customer. Being in an environment where everyone got along exceptionally was one of the best parts of working at Mosaic.

Another aspect I enjoyed at Mosaic was the fact that I was always keeping busy. Never was there a moment on the job where I found myself at my desk twiddling my thumbs. If I needed some extra work, not only did Shelby or David find me something to do, but it wasn't just busywork they would have me do. They would give me work that needed to be done to help the organization in the long run. So, all the work I did at Mosaic was important and that made me feel great about myself.

Overall, my experience at Mosaic was 10/10 and I would recommend any aspiring engineer to work for them. I learned so much about the microelectronics industry, as well as chemical engineering. Shelby and David were great at making me an integral part of the team by incorporating me in many of the meetings and allowing me to voice my thoughts and opinions on the process. Together, the teamwork we had was great and led to high efficiency in the lab, and quality products provided to the customer. I am forever grateful for the opportunity, thanks to the team at Mosaic.

From Macro to Micro: Learning Microelectronics Firsthand at StratEdge

By Louise Greco, StratEdge

Louise Greco's experience at StratEdge Corporation made her a shoo-in for the NASA Community College Aerospace Scholar (NCAS) program.

I was fortunate enough to join **StratEdge Corporation** in May 2021 as an Engineering Technician working in the semiconductor packaging industry. I am currently an aerospace engineering student at Southwestern College and transferring to San Diego State next fall. In my time at StratEdge, I have had the opportunity to work in our electronics lab assisting in electronics assembly and learning, first-hand, the process of wire bonding and die attach for large-scale production.

Before I started school for engineering, I was an apprentice welder and pipefitter at General Dynamics: NASSCO. There I worked on staged construction containerships. I worked with many engineers and architects that inspired me to go into engineering, and after that experience, I knew I was going in the right direction.

In between General Dynamics and StratEdge, I was accepted into NASA's prestigious Jet Propulsion Laboratory's **NASA Community College Aerospace Scholar (NCAS)** program. It was here that I was a winning project manager competing in their Mars rover design project, developing, and presenting our rover design to a team of NASA engineers. I met incredible peers and mentors who helped me see my potential and potential career path. The experience solidified my desire to become an Aerospace Engineer.

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Sustainability Report Card: How Does Your Company Measure Up?

By Julia Goldstein, JLFG Communications

We are in year three of a global pandemic that has changed our perspective on health, the economy, and inequality. Attitudes toward environmental sustainability have also shifted in the past two years. We experienced cleaner air resulting from just a few months of shutdowns in manufacturing and transportation, followed by an uptick in greenhouse gas (GHG) emissions and pollution as operations resumed. Manufacturers in all industries, including semiconductors, now realize that environmental sustainability needs to be a key pillar of their operations.

I've experienced the growing interest in sustainable manufacturing through increased sales of my book Material Value: More Sustainable, Less *Wasteful Manufacturing of Everything From Cell Phones to Cleaning Product*s. The book came out in April 2019 (Figure 1).

Companies want to know how their efforts measure up and how they can accelerate their environmental initiatives as they tackle ambitious 2030 goals. In the journey toward net-zero carbon emissions, how fast is fast enough? The simple answer is that while you should celebrate progress, there is always more you can and should do.

Here is one three-step process to evaluate where you stand. First, consider how you are talking about sustainability inside your walls. Second, look at what you are saying to customers, suppliers, and investors. Finally, take an honest assessment of whether your actions match your words.

What story are you telling yourself?

Honest, transparent internal communication is essential to an effective sustainability strategy. Your company might be making great strides in reducing GHG emissions or sourcing from responsible suppliers. Or you might be lagging in these and other areas. Do your employees know where you stand?

It is important to explain your sustainability goals to all employees and regularly share progress. When employees in all departments and all locations are aware of the company's efforts, they can be part of the solution. Open communication leads to better collaboration. For example, electrical engineers can work with materials scientists to design chips that consume less power. Technicians may spot inefficiencies in energy or water use. If they share their observations, they can work with management to improve the system.

To make sustainability a top priority, there must be alignment from the top down that extends throughout the company's operations. Industry leaders foster a corporate culture where sustainability is everyone's responsibility. Employees are encouraged to speak up if they see deficits or opportunities for improvement. Is that the case at your company?

When measuring GHG emissions, Scope 1 covers emissions from the company's operations. You need to get your own house in order before broadening your horizons to your industry or your supply chain. Similarly, your sustainability report card starts with honest communication inside your walls. But it doesn't end there.

What story are you telling the world?

Prospective customers want to know what products you offer and whether your specs meet their needs. But they are also likely to ask how you stand on sustainability. When they visit your company website, can they easily find the information they seek?

Your website content and the way you organize it can indicate that sustainability is a high priority. On the flip side, the lack of sustainability-related content sends the message that the company does not consider the environmental impact of its products.

When the committee was evaluating companies for the 3D InCites 2021 Sustainability Award, we examined corporate websites. We especially kept an eye out for:

- A statement on the home page about the company's values that includes a position on the environment
- A list of recent awards and certifications
- Blog posts highlighting progress toward sustainability goals
- An easy-to-find link to a sustainability or ESG page for more detailed information
- A link to download a current sustainability report prepared according to GRI Standards

Sustainability reporting is on the rise. In 2020, 90% of the companies in the S&P 500 index published sustainability reports. Reporting is not as common for smaller companies, especially those that are privately held, but the same trend prevails.

Reports present an opportunity to show the world your goals and progress toward them. Most reports address environmental, social, and governance (ESG) issues. But reports vary quite a bit in scope, format, and level of detail. You can compare your reports to those of your competitors, customers, or suppliers as a reality check.

Do your actions match your words?

Communication is important, but words and actions must match. A company culture that claims to care about people and the planet is of no use unless there is a real commitment behind it. A beautiful sustainability page on your website does not ring true if you are proceeding with business as usual regardless of the harm you might be causing.

The United Nations Sustainable Development Goals offer a great framework for progress. But merely posting them on a wall is not enough. It is helpful to choose a few of the goals where your company can have the greatest impact. Then take a close look at your current performance and find ways to make continuous improvement.

These are the UN SDGs we considered when evaluating companies for the 3D InCites Sustainability Award:

- 6—Clean water and sanitation
- 7—Affordable and Clean Energy
- 12—Responsible Consumption and Production
- 13—Climate Action

These are all relevant to semiconductor manufacturing. Blog posts in the 3D InCites Sustainability 101 series have covered all of them with posts on **GHG emissions**, **the circular economy**, **chemicals of concern**, and **water management**.

Are you taking steps to increase your positive impact and decrease your negative impact related to these SDGs? It is important to consider all aspects of your business operations around the world. It is not enough to improve one product line or factory location. That's a great start, but high-ranking companies make global changes that affect their entire company. Then they go a step further to put pressure on their peers and suppliers.

The book *Net Positive: How Courageous Companies Thrive by Giving More Than They Take* by Paul Polman and Andrew Winston is a great resource for business leaders who want their companies to do more. The **website** dedicated to the Net Positive movement features a readiness test. This tool can help you assess your current status and point to areas where you can improve.

Your company has likely taken at least the first step toward sustainability: awareness. I hope that you will develop ever more ambitious sustainability goals and work with your colleagues, industry peers, and suppliers to achieve them.

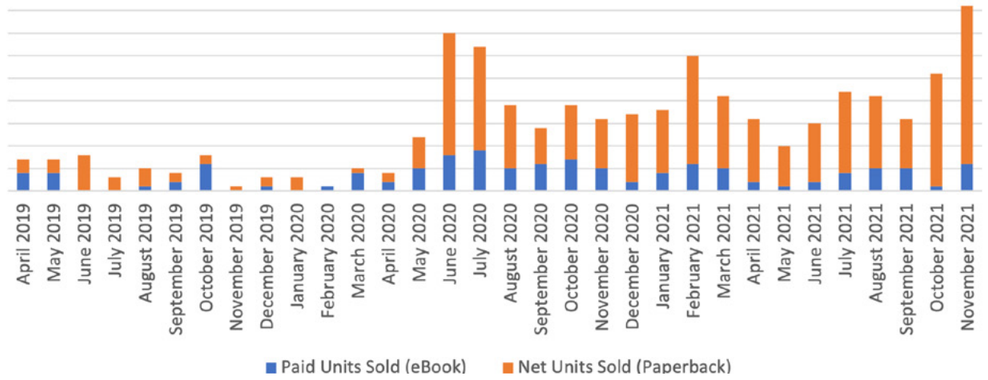


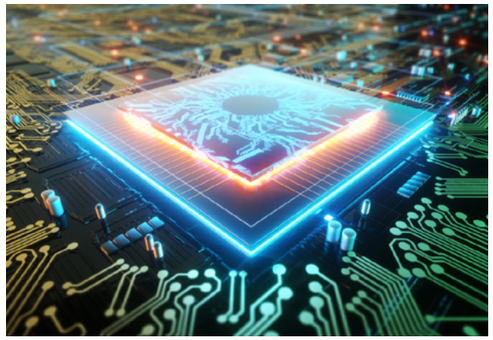
Figure 1: Increased sales of Material Value demonstrate businesses are paying more attention than they ever have to the importance of sustainability.

3D InCites Community Reflections from 2021, and What's to Come in 2022

Despite the pandemic, the chip shortage, and supply chain issues, 2021 was a boom year for the semiconductor industry. We invited our community members to share their highlights, lowlights, and Aha! moments of the year. We also asked them to take a stab at predicting what's to come in 2022. Here are their contributions.

Where Is Semiconductor Packaging Design Headed?

By Keith Felton, Siemens EDA



Here at Siemens EDA, we expect to see greater emphasis in several areas of semiconductor package design. To start, heterogeneous integration (HI) of multiple dies into system-in-packages (SiPs) will be common across all market segments and will use multiple integration platforms, not just silicon interposers, as is common today.

These complex multi-die/chiplet designs will see a greater use of hardware description language (HDL) driven flows, which speed up system definition and debug cycles compared to today's schematic-driven approaches. As these HI multi-die/chiplet SiPs grow in size and complexity, the adoption of system-level design rule checking (DRC) and layout versus schematic (LVS) verification will become mandatory to avoid fabrication and manufacturing assembly errors and their corresponding negative impact on costs and delays.

As HI-using chiplets starts to become common, almost mainstream, we expect to see the emergence of a robust supply chain of commercial off-the-shelf (COTS) chiplets containing what was previously available as soft/hard IP, as used in monolithic SoC designs. In addition, as HI SiPs become more mainstream, we will see the emergence and adoption of alternatives to silicon as an integration substrate. Organic-based interposers will deliver the wiring density and electrical/thermal performance needed for many target markets and, of course, enable larger sizes, due to no reticle limitations and lower costs.

As HI grows in usage and its available integration platforms increase, the number of die/chiplet integration permutations, or scenarios, will also grow. As a result, issues around thermal and electromechanical stress will become pervasive and will need to be understood and addressed earlier in planning and prototyping to prevent them from becoming a key problem should the wrong integration scenario be selected and moved into detailed implementation. This will drive the use of early predictive thermal and stress analysis, ideally during the planning and prototyping process, in addition to the current early SI/PI analysis. This early analysis will enable the semiconductor packaging team to identify and qualify acceptable integration scenarios and reject unacceptable scenarios.

The final area in which we will see greater focus into the next year is test. Reliance on known-good die or chiplets (KGD) by itself will not be sufficient to ensure functional performance and reliability. These designs will require the adoption of more comprehensive test strategies capable of addressing the new test challenges presented by such 2.5D/3DIC SiP designs—and by test, we mean complete, system-level test that will include the active and passive devices as well as the integration substrates and any embedded active or passive devices within them.

We expect many aspects of semiconductor package design will be considerably different sooner than later. Some will be completely new, and others will have grown or matured in their use, driven by complexity demands. In addition, an ecosystem around the supply and standardization of chiplets will have emerged, enabled by exchange formats such as those being created by the Open Compute Projects Chiplet Design eXchange (CDX) format, which will provide the catalyst for broad adoption of HI across all market segments, beyond the handful of mega IDMs/fabless and systems companies who currently have access to this capability.

Protecting Devices During a Supply Chain Shortage

By Joe Montano, Delphon

Spending 2021 as president, and with my recent appointment to President and CEO of Delphon as of January 1st, 2022, I couldn't be any prouder of my organization. Our team showed tremendous tenacity this past year. We not only survived tremendous headwinds caused by supply chain and logistics challenges but thrived, showing stellar double-digit growth over our equally excellent 2020 performance!

In 2021, we expanded our organization to accommodate and accelerate the execution of our growth strategies and have more planned for 2022. As a company, we increased our emphasis on quality and new product development.

Our goal is to provide our customers with valued solutions and become an extension of their R&D over time. This is only possible through close collaboration with select customers that share our inherent curiosity and will to solve the difficult challenges facing our industry.

Our three business units — Gel-Pak, UltraTape, and TouchMark — made it possible for us to make sure our customers' demand needs saw little or no disruption. We put a high priority on delivering an excellent customer experience, and harness that drive and desire into our creativity and problem-solving skills to consistently overcome the challenges that face us and the entire industry. It's easy during times like these to throw your hands up and use the macroenvironment to cover your shortcomings. At Delphon, we used this opportunity to show why we are best in class when it comes to protecting the world's delicate devices.

Gel-Pak launched three new products in 2021. First was our Lid-Clip Super System (LCS2™) to reduce die migration (Figure 1). The LCS2 protects extremely thin die — down to 2 mils (50µm) — from the jostling that occurs as they are handled and transported around the world by semiconductor manufacturers, their distributors, and customers.

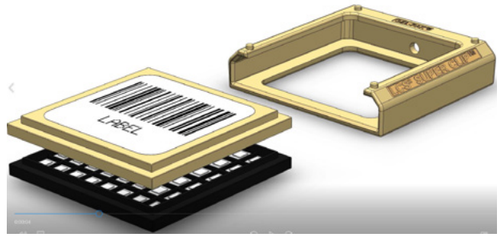


Figure 1: Gel-Pak Lid Clip Super System protects even the thinnest die

The second was APV/VRP, a non-silicone-containing polyurethane, available in vacuum release and gel box product lines, which is being quickly adopted for photonics applications, as well as others where silicone sensitivity is an issue (Figure 2).

Figure 2: Gel-Pak Polyurethane Product

Last is our unique Textured Vertec® technology, which is available in a variety of form factors and is being adopted for temporarily immobilizing devices during the manufacturing process as well as during transportation (Figure 3).

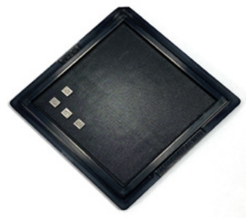


Figure 3: Vertec Textured Film on Tray

New products are always fun to talk about, but what was most important this past year was helping to keep our customers' lines up and running by ensuring that they received devices intact. We effectively managed our supply chain, at a cost, to support our existing customers seamlessly with our tried-and-true portfolio of products.

Breaking Records in 2021 Despite COVID-19

By Peter Dijkstra, Trymax Semiconductor

Trymax' new location.

2021 was a record year for Trymax Semiconductor Equipment B.V.; an all-time high. Despite the problems we encountered due to COVID-19, the order intake was very high. When COVID-19 appeared early in 2020, many companies were forced to look at their internal situation, especially their spare capacity, but also to the worldwide market situation. It was a period to decide on wait-and-watch to make drastic changes.

By the end of Q4 2020, it was clear that there would be a new way of working, i.e., whenever possible work-from-home and limited presence in traditional offices. What many people thought would be impossible, was made possible in only a few months. However, employees working from home required laptops, printers, scanners, and faster communication. All this generated a higher demand for components but in different market segments. Working from home, away from the avalanches in the office, made people also realize that quality of life (the balance between working hours and private time) is important, the environment is important, the climate protection is important e.g., electrical vehicles, this created a surge in market demand.

Trymax benefitted from this changing and increasing demand and we've seen a strong increase in IC-analog (RF filters & 5G) and discrete (power electronics) devices. Besides the change in markets, we've also gained more recognition in the market and supplied multiple tools to major OSATs, foundry services, and IDMs. In December 2021, to cope with the increase in demand for systems, Trymax moved to a new building that has more than two times the square meters of manufacturing space than its previous location.

At the same time, with multiple orders, it has been very challenging to bring out the creativity and out-of-the-box actions required due to the continuously changing environment. Multiple COVID-19 waves, a cyber-attack at a major supplier, and a shortage of components imposed risk to manage multiple orders at the same time. Hats off to the Trymax manufacturing, logistics, planning and customer support team to have satisfied all our customers.

As the COVID-19 virus is mutating, I'm convinced that 2022 will be another year in which we have to demonstrate our ability to adapt to situations and deliver our targets on time. Finally, I would like to share, on behalf of the whole Trymax team, our sincere sympathy to all who have encountered personal inconvenience caused by the COVID-19 virus. For now, stay safe!

Making the Impossible Possible: Building a Better Future After a Year of Surprising Growth and Rising Demand

By Michael Plisinski, Onto Innovation

The new year is always a wonderful time to take a deep breath, hold it and reflect on the past 12 months while planning for the year ahead. In the semiconductor industry, we have never seen a year like 2021, one with so many surprises combined with so much growth.

In 2021 we saw semiconductor manufacturing expansions accelerate across the value chain. Advanced logic was especially pronounced, with leaders seeing the opportunity to serve the growing market for high-performance compute or hyperscalers to power artificial intelligence (AI) engines in a wide range of applications. But 2021 will be remembered for broad demand growth, with 5G adoption in mobile handsets and base stations continuing to double each year. This drove a strong surge in the introduction rate of next-generation mobile handsets, which ushered in higher demand for camera chips, power, and memory.

In addition, the industry managed through national concerns about semiconductor technology challenges from the ongoing pandemic, and, as a result of the sharp increase in demand, a worldwide supply chain shortage of chips compounded by logistics challenges around the globe.

Against this backdrop, companies like Onto Innovation will see a growth of 40% year over year, and demand is continuing to rise in 2022. All the drivers are the same for the new year as in 2021, but we also see an increased focus on compound semiconductor devices, particularly for power devices supporting the global emphasis on transitioning from the 130-year-old combustion engine to electric vehicles (EVs) and the world's critical need for smarter power grids that allow more renewable energy sources to come online. Along with that, we project higher levels of investment in heterogeneous packaging technology for 2022 to support the next generation of AI engines and high-performance integrated modules, such as those for 5G communication.

But there will be challenges as well. The pandemic remains with us. Although logistics should begin to improve, supply chain challenges due to chip shortages will likely take longer to resolve, and we have inflationary pressures that are creating challenges for companies on several levels. However, as we have demonstrated in the last two years, this is a very resilient industry made of companies staffed by passionate, talented, and creative people that work together across company boundaries to make the impossible possible. It's what we do.

Onto Innovation is proud to play an increasingly more important role in our industries' success and contributions to a better world. That improvement is not just in the products we enable, it's in our efforts to work in our communities to create opportunities to introduce under-represented groups to the fields of science and technology at an early age. It means ensuring we have flexible workplace policies that enable people of all backgrounds to be their best when they have different demands and pressures.

In the end, our success as a company is directly attributable to the successes of the individuals who make up our team. At Onto Innovation, our employees are our competitive advantage. We look forward to seeing our company, the industry, and the world grow to meet a better future in 2022 and beyond.

Another Strong Year Ahead for Hybrid Bonding Thanks to Heterogeneous Integration

By Thomas Uhrmann, EV Group

While the COVID-19 pandemic has continued to cause mass disruption to the global economy during the past year, one notable bright spot has been within the semiconductor industry, where fab spending in new process equipment reached a new record high of more than $100B according to SEMI. This spending growth was driven by both capacity expansion as well as investments to ramp up new process technologies into production. For EV Group, this has meant investments across the board in our wafer bonding, lithography, and metrology solutions, particularly those supporting 3D/heterogeneous integration and photonics manufacturing.

Besides seeing continued strong demand for our products, EVG also continued to see strong demand for our process development services, including those through our competence centers for heterogeneous integration and photonics. These innovation incubators enable us to work closely with partners and customers to help them develop new integration and device applications in these segments. Joint development agreements with Applied Materials and ASMPT involving wafer-to-wafer (W2W) and die-to-wafer (D2W) hybrid bonding, respectively, are just a few examples of our collaborative partnerships in heterogeneous integration. Our continued work with SCHOTT, Inkron, and others in developing high-volume manufacturing solutions for high refractive index waveguides, our work with ZKW in dynamic light projection technology leveraging micromirror MEMS type devices, and other partnerships, are helping to drive innovations in photonics for automotive, industrial and home entertainment applications.

Many industry analysts expect 2022 to be another strong year for semiconductor process equipment suppliers. We believe that heterogeneous integration will continue to be a strong driver for the industry due to the relentless pursuit of bandwidth scaling to support new industry megatrends such as high-performance computing (HPC) and artificial intelligence (AI). As many know, bandwidth scaling is closely tied to interconnect scaling.

With tighter pitches between interconnects, more connections can be achieved within the same area on the device, which in turn means that more data can be transmitted. Higher bandwidth needs are driving newer packaging technologies. The transition from 2.5D to 3D SIC packaging, and from 3D SIC to 3D SoC packaging, can provide several orders of magnitude improvement in bandwidth. However, these new packaging technologies have tighter pitch requirements, which in turn drives the need for new and different hybrid bonding techniques.

W2W bonding processes are enabling new device fabrication concepts, such as memory-on-logic devices through the transfer of memory layers like NAND, DRAM, SRAM, or Flash from one wafer to another, as well as backside illuminated image sensors and other heterogeneous integration device applications. Improving overlay between wafers during W2W bonding enables the connection of different layers at earlier metal levels, which saves cost as well as increases device bandwidth and performance. For the production of the first generation of image sensors around a decade ago, W2W overlay in the range of 500nm to 1µm was sufficient. This has quickly scaled down with future device generations. Today, W2W overlay requirements for leading-edge applications today range from 500nm down to 100nm overlay pitches.

In D2W bonding, the dies, as well as the carrier/target wafers, typically have alignment patterns, which serve as fiducials for both patterning and alignment verification after full population. As hybrid bonding targets interconnect pitches from about 10µm down to 2µm in the future, the same scaling needs to happen for the placement accuracy as well as the metrology to control and yield the process. For future roadmaps targeting 2µm interconnect pitches, a factor of 10X improvement is required for placement accuracy and metrology precision (20nm for each).

While advancements in bandwidth and packaging are driving tighter specifications for hybrid bonding, EV Group is up to the challenge. At the center of our product roadmap is our emphasis on increasing product performance and maintaining flexibility in our product platforms to support our customers' wide-ranging and ever-evolving requirements. In addition, our collaborations across the supply chain allow us to share data and learn from different areas of strength, which leads to better support for our customers in solving their critical manufacturing challenges.

Wafer-Level Packaging Is Well-Positioned for Growth

By Sally-Ann Henry, ACM Research

Wafer-level packaging (WLP) saw significant growth in 2021 due in large part to the increased performance needs of data-driven 5G network devices. Because WLP is performed when chips are still on the wafer, ACM Research has been able to leverage and adapt our expertise in front-end solutions to address high-volume WLP challenges. Our deep understanding of new and emerging requirements has enabled us to exceed customer expectations over this last year, and we're looking forward to continuing our momentum in the years to come.

One of the primary ways we've addressed WLP requirements is by increasing our ability to serve the global marketplace. Throughout 2021, we've grown our U.S. and European teams to meet changing market needs, and we plan to expand our team further in 2022. ACM has also received several orders from major U.S. manufacturers, demonstrating our successful globalization strategy. We've been chosen by these manufacturers for our proprietary and differentiated technologies, as well as our ability to meet advanced performance specifications. All of this led to us being recognized as the eighth-fastest-growing organization on Fortune magazine's 2021 100 Fastest-Growing Companies list.

As is true for the semiconductor industry at large, we've faced challenges from global supply chain issues in 2021. At the same time, this shortage is creating a significant opportunity for equipment suppliers like ACM. As the world's need for chips has exploded, supply chain disruptions have made it difficult for chipmakers to meet demand. This is driving large manufacturers to add capacity and build new fabs to address chip shortages—and new fabs need new equipment.

As we move into 2022, we predict both the front-end and WLP markets will continue their rapid growth. We plan to maintain our momentum by continuing to add to the range of process technologies we support. For WLP, we currently offer thick photoresist coating and developing, EC plating, metal etching, and resist stripping for redistribution layer through-silicon vias and bumping processes. Our WLP systems support copper pillar and gold bumping as well. Looking ahead, we will assess market demand and continue to deliver advanced technologies that extend our portfolio, both in terms of processes and markets served.

Just as our core markets are growing, ACM also has ambitious growth plans. We're hiring across the globe, developing new technologies, and, importantly, we're focused on reducing chemical usage and waste. ACM is dedicated to helping customers reach their sustainability goals, including zero-waste-to-landfill initiatives. As part of this, we've developed closed-loop systems that require lower chemistry volumes and recycle-and-reuse chemistries for eco-friendlier processes.

Allied Market Research predicts the global WLP market will reach **$7.8 billion by 2022**, and ACM is on track to lead the way.

Staying Ahead of the Advanced Packaging Technology Curve

Rezwan Lateef, YES

Advanced packaging technology enables continued performance scaling across applications, and it is clear that the coming generations of mobile and edge computing, cloud computing, and distributed high-performance computing will require heterogeneous chip integration technologies. To accommodate demanding performance and scaling requirements while also meeting stringent technical specifications for speed, bandwidth, power delivery, and thermal management, leading-edge devices will depend on multiple passivation layers and redistribution of metal routings to connect the various chips.

One of the world's largest mobile phone companies adopted wafer fan-out PoP packaging technology back in 2016 to address these issues and not surprisingly, additional companies have been following suit. Another mobile phone giant has announced that it is developing its version of FO-WLP for mobile applications, while simultaneously working on yield improvement and cost reduction with the use of panel fanout.

As wafer fanout technologies evolve, several of our customers are starting to adopt interconnect bridge technologies, which offer several advantages. By providing high density, the bridge allows relaxed feature sizes for redistribution layers (RDL) and improves yield. Using a bridge can also allow a reduction in the number of RDLs, thereby reducing the cost of the package.

Concurrently, the package size is also evolving. While the most common substrate package size is still 35x35mm, we have seen next-generation multiple chip integrations with package sizes as large as 150x150mm.

To stay ahead of the technology curve, we at YES work in close partnership with our installed base of semiconductor industry leaders, ensuring that our products meet their current and future technology needs, both for smaller form factors and high-performance applications with larger areas supported by high-density laminate and glass-based substrates. Toward that end, we are working on issues such as solder reflow in reducing environments for small pitch BGA and ensuring that our panel-based VertaCure™ and VertaBond™ systems address the unique surface enhancement needs of larger substrates.

As a further step in our ongoing mission to enable our customers' roadmaps, we recently acquired Semiconductor Process Equipment Corporation (SPEC) of Valencia, CA – a highly-regarded manufacturer of wet processing equipment. SPEC's high-volume electroless plating systems for under-bump metallization, along with its decades of expertise in critical advanced packaging technologies like electrolytic plating, will enable YES to maintain our leadership in enhancing surfaces and materials for our customers' applications.

We predict that chip-to-chip interconnects, performance, form factor, and power delivery demands will continue to drive the adoption of RDL-based solutions, and we look forward to meeting the challenges of this exciting era for advanced packaging.

The Foundation is Set: Ready for Growth in 2022

By John Voltz, Reno Sub-Systems

It's been a wild ride in the semiconductor industry in 2021! The continued push toward smaller dimensions and new technologies like heterogeneous integration and chiplets, and more generally, the chip shortage, have spurred significant investment globally. Reno Sub-Systems has been front and center in both areas throughout the year.

Our Velocity™ RF matching network technology took off in terms of sales this year. We received the largest order in our history in the fourth quarter, after booking multiple orders throughout the year—and winning two new design-ins—as our approach to RF matching is quickly becoming mainstream for next-generation plasma processing.

We continue to lead the industry in technology development, launching our GenMatch™ integrated RF power systems (Figure 1). The GenMatch™ Series integrates our proven solid-state Electronic Variable Capacitor (EVC™) RF match and Precis™ RF generator technology into a single unit. This saves space on the process tool, and is faster, more repeatable, and more reliable, with a lower cost of ownership.

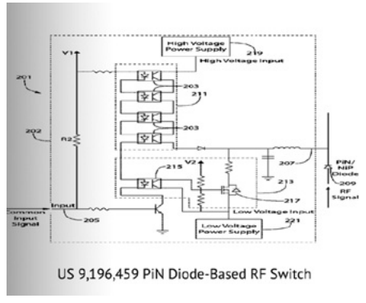
Another key focus for the company has been expanding our intellectual property portfolio, which is key to retaining our leadership position as device manufacturers move to smaller process nodes (Figure 2). In 2021, we secured 10 new patent (Figure 3). With these additions, Reno holds 45 patents in total, which is the world's largest solid-state patent portfolio for RF matching networks and RF generators. As we continue to broaden and strengthen our IP portfolio, it limits the possible alternatives to design a solid-state matching network not covered by our IP.

As was true for many companies in the industry, growing demand has driven new opportunities in engineering, test, and build. We expanded our New Jersey facility last December, and 2021 has been a year of hiring to support our growth. We were also pleased to welcome two new board members to Reno in Q1 of this year: Jeff Andreson and Jorge Titinger. Both have been instrumental in supporting us and helping to chart our path through the current market.

So, what does the future hold? VLSI Research's John West, whose report on **semiconductor equipment power subsystems** was published in July, supports our market expectations and forecast for rapid growth. We believe RF generators and RF matches represent a significant portion of the power sub-systems market addressed in the VLSI report. The combination of growing adoption of our technologies across a wide range of advanced processes—including ALE and ALD—and the momentum of current processes moving into high volume manufacturing at multiple sites, leaves us excited about the prospects for growth.

Current predictions are for growth at least through 2023 to address the continuing chip shortages. This will continue to drive a strong equipment business alongside technology development, and increasing the number of die per wafer will help meet growing demand globally. This push to smaller nodes will strengthen Reno's business, and we anticipate another record-breaking year in terms of sales. What a wonderful time to be in the semiconductor equipment business!

Figure 1: GenMatch™ Series



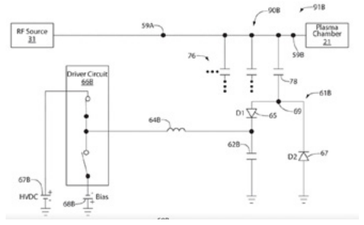


Figure 2 & 3: Our patent portfolio expands again!

From Chaos to Opportunity

Patricia MacLeod, ASE

ASE, Inc. CEO, Dr. Tien Wu, has often referred to Sun Tzu's legendary quote when describing semiconductor market volatility, "In the midst of chaos, there is also opportunity." This rang particularly true over the past few years. Undoubtedly, the semiconductor chip emerged heroic from the chaos of pandemic times, underscoring its relevance and impact on 21st century life, particularly as digital transformation kicked into high gear. But in the glaring global spotlight was the semiconductor industry itself and the supply chain disruption that caused unprecedented effects to ripple across society.

We are well on our way into 2022 now, a year holding much hope for innovation that can truly create improved realities across our interconnected world. At ASE, we're taking stock of who we are and how we will innovate technologies for the greater good. That requires reflection on the year gone by and perspective on what's ahead. I recently asked some ASE's executives for their thoughts:

Mark Gerber, Sr. Director of Engineering and Technical Marketing, surmised, "This last year has brought exciting new technology advancements within the packaging ecosystem. Heterogeneous integration has gained interest across all market segments, which has driven many new package structures that support greater integration, improved performance, and optimized silicon yields. Supporting technologies such as hybrid bonding, advanced redistribution layer and chiplet/passive integration are a few examples of leading-edge tools that ASE is using to further enable our customer products."

Echoing Gerber's thoughts that metaverse boom and 5G-NR roll-out will escalate demand for higher performance solutions around digital, RF and analog systems, is Sophia Djurovic, Director of Business Planning, "Leading industry analysts are very focused on how the metaverse is driving significant innovation across augmented reality and virtual reality, compute, server, and artificial intelligence (AI)."

With his take, Eelco Bergman, Sr. Director, Business Development, commented, "The Age of Chiplets has truly started, cemented by product and production start announcements from leading suppliers. He continued, "We believe that adoption of chiplets will drive the industry to evolve from silicon-centric thinking to system level planning, and place crucial focus on co-design of IC and package. Heterogeneous Integration will play a vital role in bringing chiplet-based designs to market."

Ou Li, Sr. Director of Engineering, described how the 2022 technology buzz across packaging and application can be attributed to, "MEMs and sensors for wearable and Internet-of-Things, Power devices for the automotive industry, wafer level packaging and flip chip for mobile and consumer industries, and 2.5D/3D and system-in-package (Sip) innovations for data center, cloud computing, AI and 5G."

ASE Fellow and Chair of the Heterogeneous Integration Roadmap (HIR), Dr. Bill Chen, visualizes a clear path ahead for Heterogeneous Integration given its impact on innovation around chiplets, high performance computing (HPC), and AI and machine learning (ML) , augmented by opportunities on the innovation horizon for autonomous automotive and beyond 5G.

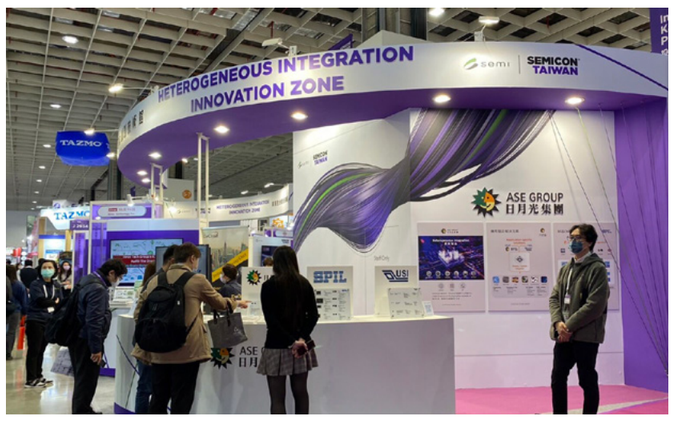
Initiatives related to sustainable manufacturing remain high priority, with Sr. Director of Corporate Communications, Jennifer Yuen, pointing out, "As focus on ESG strategy within the semiconductor industry intensifies, ASE continues to step up by implementing innovative measures as part of our commitment to a win-win sustainable future and reaching towards our low carbon, circular, inclusive, and collaborative goals."

Our industry's future has never been brighter. The metaverse is going to be a big part of our future and, as we progress into 2022, it's important to understand strategic and portfolio implications. After all, semiconductor chips literally form the brain of every single electronic device currently transforming our world. As part of this complex ecosystem, ASE is innovating to ultimately help deliver the compute power and system performance necessary for a safer, healthier, and more sustainable planet.

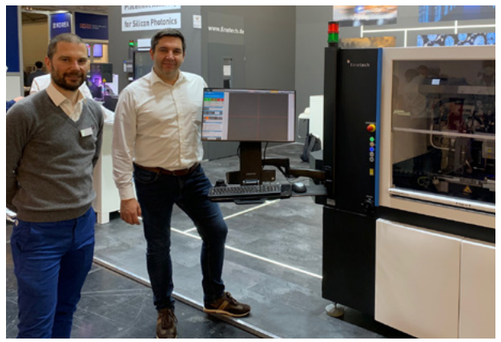
2021 IN PICTURES

IMAPS Symposium

SEMICON Taiwan



SEMICON Europa



SEMICON West

IFTLE 500: We've Come a Long Way, Baby!

Continued from page 15

Len Schaper, Eric Beyne, Michael Toepper, Paul Van Loan, Pete Singer, Peter Ramm, Mitsu Koyanagi, Bill Chen and so many, many more.

- IFTLE also thanks Alan Huffman and Chris Bower whom he has tried to mentor through the years. It might be arrogant to call them protégés, but I'll do that anyway! (Figure 6)

Consolidation is a natural occurrence in all manufacturing genres. In the last decade, consolidation has occurred throughout the advanced packaging supply chain. This was evidenced by watching front-end equipment suppliers, AMAT, TEL, LAM buying up smaller back-end packaging equipment suppliers.

Watching the IC community attempt to move to 450mm and fail and watching Moore's law and scaling slowdown has reinforced the old saying that "all things must come to an eventual conclusion".

The 2014 sale of IBMs NY fabs to GlobalFoundries summoned the end of IBM as we knew it.

In 2009 I predicted to a group of Government agencies that IBM would soon be out of the IC fabrication business due to the evolving economies of IC fabrication. I was laughed off the stage then…but who got the last laugh?

Would any of us have ever predicted the demise of DEC, Motorola, IBM, NEC, Hitachi, or Fujitsu as IC giants?

IFTLE has been fascinated by buzzword evolution whether it be "multichip modules" or "internet of things" or "wafer-level fan-out" or "nanotechnology" or "3DIC" or most recently "chiplets". Especially watching all the secondary and tertiary players in the ecosystem trying to develop their "spin" to attempt to sell their technology as fitting into distorted definitions of these buzzwords.

What I have seen over the years is that the bigger the technology's ultimate success, the more naysayers there were initially predicting those developments would never happen. Specifically, I can call out bumping, wafer-level packaging, hybrid bonding, chiplets, and oh so many more. Those entrenched in the old classical technologies say "Never going to happen" but technologies that serve a need can never be kept down for long.

Specific Technology Predictions

Although fan-out WLP was a natural evolution for WLP, who in 2006 would have predicted that Infineon and its e-WLB process would win out over Freescale and its redistributed chip package (RCP)? e-WLB licensing to ST Micro, ASE, StatsChipPAC, and many others settled that question.

A plethora of technical issues evolved as the community attempted to commercialize 3DIC such as:

- Eric Beyne's IMEC group solving the copper extrusion issue
- Brewer Science developing numerous new products to meet the evolving requirements of 3DIC temporary bonding
- In the early days of 3DIC, it was unclear who would own the processes to create TSVs. The more we learned about "vias middle" technology the clearer it became that TSV were meant to be introduced front end in the fab and not back-end in the assembly houses
- Watching Qualcomm, at one point the strongest corporate advocate for 3DIC in the world, (Matt Nowak, Riko Radojcic, Liam Madden, Steve Bezuk) pull the plug a bit too early on their 3D efforts. While unfortunate, this is expected when a company enters a technology too early and has to carry those costs over an extended period
- While Micron and its hybrid memory cube (HMC) consortium got all the early hype, it was Hynix who took high bandwidth memory (HBM) over the finish line to become today's gold standard in stacked memory. (Samsung and Micron belatedly followed.)
- The amazing work that Doug Yu and his team at TSMC have done on advanced packaging (**CoWoS**; **InFO**; **SoIC**)
- Xilinx 2011 introduction of Vertex-7 FPGAs using disintegration and silicon interposers (Suresh Ramalingam et. al.) as the forerunner to today's chiplet technology.
- Amkor's mainstreaming of copper pillar bump technology
- 3DIC stacking becoming the main technology for advanced CMOS Image sensors mainly due to the technology of Ziptronix and the outstanding development work of Sony
- Bryan Black came out at the Georgia Tech Interposer Technology Workshop in 2011 and stated that AMD was moving to a 2.5D and stacked memory approach…our first exposure to what we now call chiplet technology
- Industry confusion over the definition of "3DIC integration" and then even more confusion (extending to this day) over the definition of chiplet technology
- Watching typically front-end processes such as lithography and CMP become standard packaging tools. Today's advanced packaging house must have this capability in their repertoire if they are doing advanced packaging
- IFTLE is amazed that while the use of metal lead frames and wire bonding has become passe, mold compound has managed to maintain its position in today's leading packaging applications
- Watching the re-emergence of what we used to be called "large-area processing" into "panel-level processing"
- Watching the transformation of multichip module technology, MCM, of the 1990s into the system-in-package (SiP) technology of the 2000s
- Watching Ho-Ming Tong coin the phrase " 2.5D" in 2009 saying that ASE was not quite ready for 3D. What was initially a joke became a standard genre of advanced packaging.
- Watching Corning, Schott and Asahi Glass try to bring glass substrates into the mainstream of IC packaging. It has not happened yet…but maybe it will.
- Watching traditional underfill evolve into NCP and NCF
- Watching transfer molding evolve into compression molding.
- As we move to more and more modular partitioning, watching warpage becomes one of the most important things to control in advanced packaging.

I could go on forever, but I won't…you get the big picture.

What started with Bob Nowak and Don Dix of Dow Chemical saying to me in the mid-1980's "Your job is to get us into materials for microelectronics" created a career path for me that has allowed me, at this point, to share my thoughts with the worldwide packaging community. What more could a techie ask for?

A review of IFTLE 500 would not be complete without mentioning that being "old school" and proudly never having been accused of being "politically correct" I don't do social media. You will never find me on Facebook or Twitter. My only dabbling in "sharing" personal info, however, has been sharing a pictorial history of my granddaughters growing up with my PFTLE/IFTLE readers (Yes I know …that's what grandparents do!)

My first picture of Hannah and her little sister Madeline appeared in 2008. The readers' favorite photo was Halloween 2010. Hannah is now 5'11", medaled in the 2018 Jr Olympics in the 4×400, and is equally academically accomplished. She will be heading off to college next fall with Madeline following a few years behind. When I am gone, I'm assured that they will carry on admirably (Figure 7).

Lastly, I don't exactly recall when the editorial advisors of Advanced Packaging were assigned caricature photos but when I saw mine, I loved it and henceforth have used it for all matters private and public. Hannah and Maddie call it "cartoon grandpa" It's kind of a reverse of the "portrait of Dorian Gray" theme. While I get old and wrinkly, the caricature does not. This certainly is the way I want to be remembered.

So, as Bob Hope used to say "Thanks for the memories". Here's to IFTLE 500. I don't know how many more will come. I'm now well past retirement age but why retire when you're still having fun!

Figure 6: Phil and friends through the years.

Phil's granddaughters, Hannah and Madeline, through the eyes if IFTLE

Adaptive Control: The "Holy Grail" in Semiconductor Smart Manufacturing

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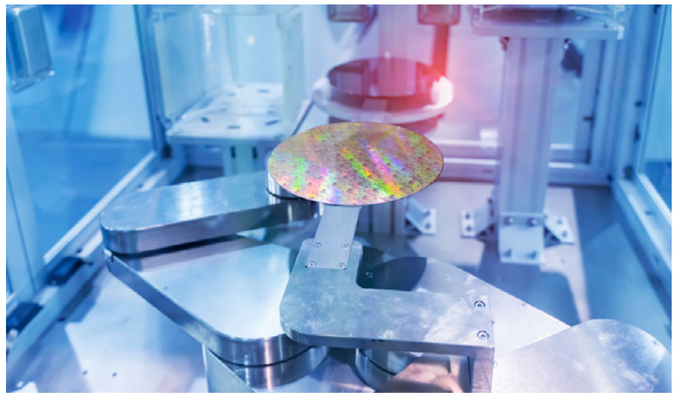
the platform to support edge to hybrid-cloud deployment topology for easy integration with third-party technologies.

As such, global enterprises can easily integrate their digital transformation technology ingredients such as data virtualization and unsupervised learning on the edge, and transfer learning between machines, manufacturing lines, and geographically distributed sites in a scalable, flexible, and cost-effective manner. This allows the customer to be cloud-agnostic and accelerate innovation to achieve tangible transformational business outcomes.



The inferencing models capture, store, and analyze real-time data at the edge, delivering predictive data intelligence for production environments in milliseconds. The time-triggered architecture can predict, at the millisecond level, whether data readings monitored are within a permissible range, for example. If data goes out of range, several different reactions can be triggered. It puts the customer back in control of their production systems without the need for costly systems integration and time-consuming IT implementations. Once the ML models have become mature, with the customer's approval, the platform can work directly with the machine itself for adaptive control and optimization.

Applications

The AI/ML platform can be quickly deployed - in most cases providing same-day access to critical system-level data that, working with the ML models to be developed for several weeks, enables the customer to predict equipment degradation, prevent faults, reduce unplanned downtime, and improve asset health and utilization. The platform enables customers in the semiconductor industry to transition from relying on reactive maintenance strategies to predictive monitoring and control of their end-to-end operations, often with increasingly complex machinery and systems. The no-code/low-code solution can be deployed quickly and easily, and scale as the needs grow. Further, the platform not only performs predictive analytics on manufacturing equipment but also can test and control it remotely, if needed.

Observability, visualization, and traceability can all be realized from the site or line-level down to the machine sensor level, with granularities unimaginable before, offering unprecedented insights and intelligence for optimization and continuous improvements. The ML models, through continuous refinement in real-time, are used for predictive maintenance (by anomaly detection) and more importantly, for adaptive control of the machine and process directly.

These capabilities have been leveraged by several large global enterprises for semiconductor fab, advanced packaging, fiber optics for transceivers, precision placement for SMT, and other challenging processes, with significant improvements in process yield, while reducing cycle time and machine downtime. This is particularly helpful when there is a capacity shortage in the semiconductor industry. For example, a large, multinational semiconductor company deployed the AI/ML platform to manage its microdevice assembly production line. All equipment motor axis movements, component gesture movements, and subsystem positions are tracked every 25 milliseconds to minimize any unplanned downtime. The software platform runs locally at the customer's facility to maintain data security from external risks and to ensure ultra-low latency program execution times.

As the platform is machine agnostic, it can be deployed onto various machines on the line across the factory. This is particularly powerful as upstream and downstream machines can now "collaborate" for overall synchronous optimization. Complex models that involve multivariate relationships between data sources, operating in-situ – at "process speed" – can be delivered.

Conclusion

There are many potential AI/ML applications for intelligent edge automation in smart manufacturing for semiconductor fab, advanced packaging, assembly, and test. It is a critical tool to enable innovations in the industry as advanced technologies demand increasingly more complex manufacturing processes.

Through The Eyes of Our Interns

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At StratEdge, I'm assigned to our Engineering Development team to assemble their new high-frequency QFN packages and to assist in developing an efficient building process to increase production yields. This project involves a lot of fine motor skill practice considering its challenging size of 4mm x 4mm, which can only be seen clearly under a microscope. But with the help of my coworkers, I was able to learn the skills required very quickly.

At StratEdge I have learned many skills from all stages of our production, from screen printing the parts to plating, assembly, wire bonding, and testing. That range of exposure can be difficult at larger companies, and I've enjoyed a fast-paced, innovative environment.

I am very grateful to have a team that trusts me to play such a significant role in the company. As an engineering student, it is exciting to have real-world problems to solve, and ultimately build my confidence for my future as an Aerospace Engineer.

How My Internship Gave Me Hands-on MOCVD Experience

By Dolores Termini, Veeco

My name is Dolores Termini and I started as a full-time Applications Lab Intern at **Veeco** this past summer and continue interning part-time during the fall semester. This internship has helped me broaden my knowledge base of semiconductors, metal-organic chemical vapor deposition (MOCVD), and material characterization thus far. As someone who does not have a direct background in any of these fields, the experience has been new and exciting.

With an undergraduate degree in optical engineering, I was able to apply some of my knowledge and understanding to the characterization tools used to help characterize wafers with different devices. Some of the characterization techniques I have learned about and have used include ellipsometry, atomic force microscopy (AFM), x-ray diffraction, electro-luminescence mapping, and optical microscopy.

For example, I was able to use ellipsometry to determine the thickness of aluminum nitride (AlN) films on a few wafers which helped with the development of an MOCVD recipe. I also used AFM to see the topography of wafer surfaces which helps us see hillocks and pits that appear on a wafer's surface which could indicate a problem with crystal growth leading to a change in MOCVD recipes for that specific device.

Dolores Termini appreciated the hands-on experience she got at Veeco during the pandemic.

In addition to using characterization tools that already exist, I was working with one of Veeco's scientists on a new optical setup to identify slip lines in wafers. We worked together to cross-reference the parts and components that we had with ones that we needed to minimize. Based on these facts and my knowledge of optics, I was able to make a Solidworks assembly of the setup to understand the spacing of all the components. From this, we created a bill of materials to determine the price. This was my first experience pricing a setup and using Solidworks so extensively. It was great to see how the knowledge I already had could be used in different, and sometimes unexpected, ways.

Since the COVID-19 pandemic started, I was not able to perform these lab measurements until I became an intern at Veeco. My lab classes were unable to meet since I was an online student for the last year. This internship has helped me get hands-on experience with tools that I had learned about but was never able to use in person due to COVID restrictions at school.

Already during my first couple weeks as a graduate student studying material science, I can see that a lot of the work I have done at Veeco is extremely applicable to my classwork. Transitioning to a slightly different field for graduate studies can be difficult but this internship has helped me learn a lot of meaningful background when working with scientists and lab technicians. This has been a great opportunity thus far and I look forward to how I can learn more about MOCVD and semiconductors.

Vehicle Electrification Driving Supply Chain Evolution

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Conclusion

Backed by the strong electromobility trend, the automotive power module market is expected to see a compound annual growth rate (CAGR) of 25% from 2021 to 2026 [3]. With high performance and high-reliability semiconductor technologies readily available, the design and cost of power modules could become a differentiation factor for automakers and their Tier1 suppliers. At the same time, there is a strong desire from vehicle manufacturers and Tier 1s to create a transparent and shortened supply chain. As a result, both of these groups should focus on co-development efforts and partnerships directly with OSATs to accelerate go-to-market timelines and provide sustained profitability.

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