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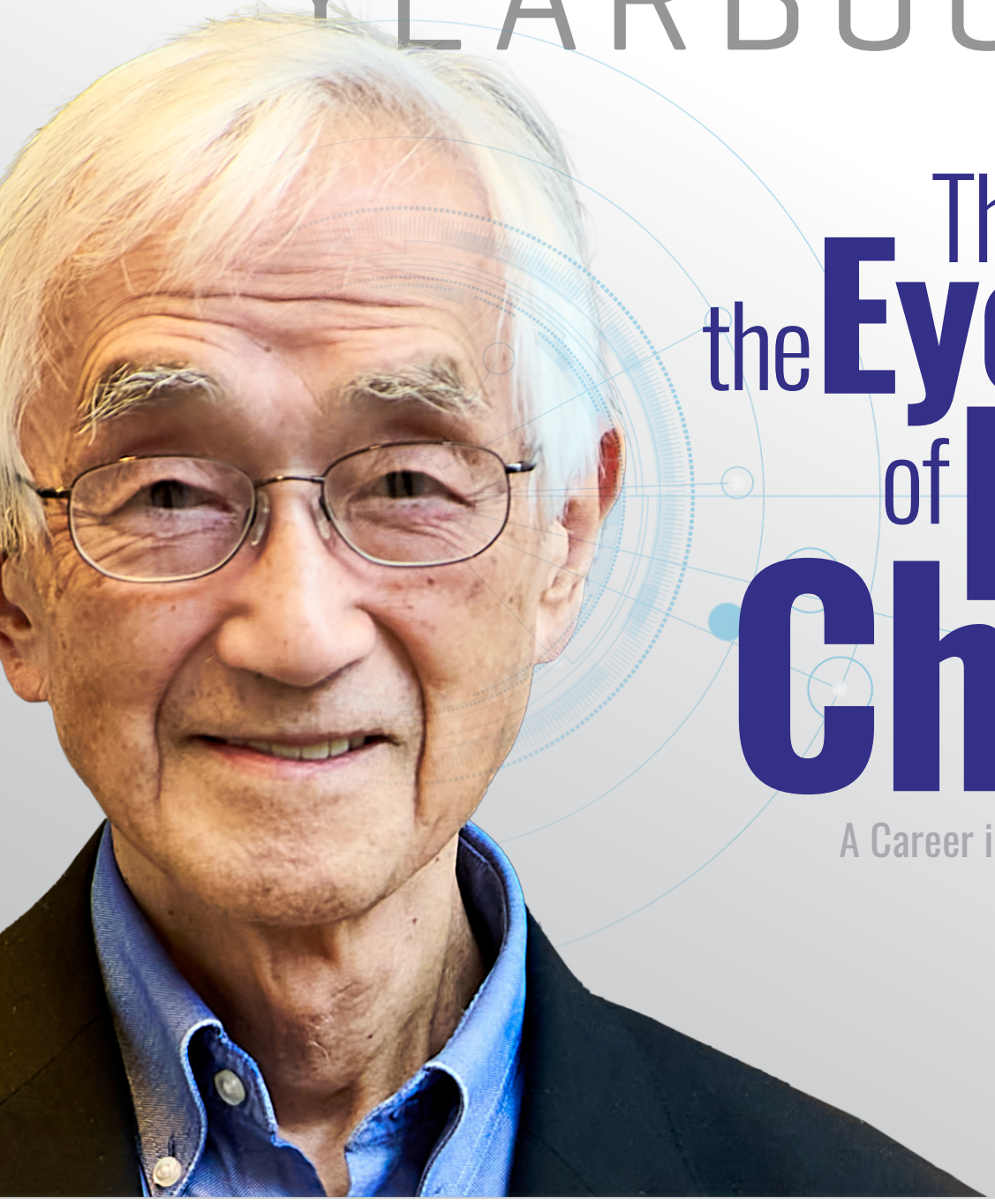

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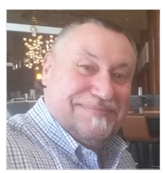

Keith Felton, author of, *The Rise of Organic and Glass Substrates,* is the Marketing Manager for the Xpedition IC Packaging solutions at Siemens, driving the strategy and direction for multi-substrate prototyping, design, and verification solution for high-density advanced packages. He has worked extensively in the area of IC Package design since the late 1980s. In the early 2000s, Keith drove the launch of the industry's first dedicated system-In-package design solution. In 2017 he led a team that launched Mentor's OSAT Alliance Program. Prior to Siemens, Keith was Group Director of Product Marketing at Cadence Design Systems.

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Stephen Hiebert, author of *Heterogenous Integration Moves to Another Level Using Hybrid Bonding,* is senior director of marketing for the LS-SWIFT Division of KLA Corporation's Semiconductor Process Control Group. He is responsible for driving business initiatives in the advanced packaging and optical devices market segments. With over 20 years at KLA, Steve's experience spans product and strategic marketing for wafer inspection and metrology as well as corporate marketing roles.

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John Park, the author of *Building a Chiplet Ecosystem,* is the Product Management Group Director for Advanced Semiconductor Packaging at Cadence. He leads a team responsible for defining cross-domain solutions and methodologies for IC, package, and PCB co-design and analysis. He is especially focused on developing tools and flows for chiplet-based 3D designs. He has over 40 years of experience in the EDA field and is regarded as an international expert on chiplets, packaging, and heterogenous integration. John has given many conference presentations, done webinars and speeches, and written several articles.

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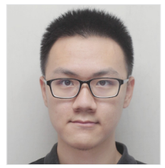
Audra Koch, the author of *Cross-disciplinary Experience is Key to Intern Success,* spent the summer of 2022 as a machine learning intern at Brewer Science. She is currently a graduate student in computer science.



Wang Yinghao, the author of *Finding an Engineer's Sense of Achievement at KLA* grew up in China, always knowing he wanted to use science to design solutions for societal and industrial challenges. He interned at KLA for 11 months, ending in August 2022. Currently, he is a junior studying mechanical engineering at Imperial College, London, United Kingdom

2022: A Year of Chips Acts and Chiplets

By Françoise von Trapp

2022 will be remembered as a rollercoaster ride for the semiconductor and microelectronics industries. After several years under the COVID-19 cloud, we started to see breaks in the storm. Analysts were optimistic that despite the geopolitical headwinds, we were back on track to become a $1 Trillion industry in the next 10 to 12 years. But then, the war in Ukraine, the geopolitical situation in China and Taiwan, the ongoing chip shortage, and an impending recession had analysts revising their optimistic outlooks as the year progressed. But none of that seems to be dampening the excitement that came along with introduction of the EU Chips Act in February and the passing of the U.S. CHIPS and Science Act in August.

In the U.S., Arizona is gearing up to become the new epicenter for semiconductor and microelectronics manufacturing, as construction on both Intel's new fabs and TSMC's gigafab are well underway. We are excited about this, as our headquarters are in Phoenix. Many 3D InCites members, including Amkor Technology, Inc., Deca, Finetech, EV Group, EMD Electronics, Kiterocket, and Mercury. Additionally, YES and our newest member, Edwards Vacuum, each unveiled plans to open new facilities in Chandler.

Our European members are equally enthusiastic about growth, as the EU sets its goal to double its market share of global semiconductor production from 10 to 20 percent by 2030. Steffen Kröhnert, ESPAT-Consulting, represents 3D InCites in Europe and has his ear to the ground on what's happening in the advanced packaging space there. At SEMICON Europa 2022, he moderated a panel discussion on the topic. You can listen to the entire conversation as a podcast **here**.

For our annual Community Reflections article, we asked our members how the EU Chips Act and U.S. CHIPS and Science Act impacts their business. Mosaic Microsystems, YES, EV Group, and Trymax Semiconductor share their stories **here**.

The other hot topic of the year was chiplet architectures – how to build them, what challenges remain, what technologies enable them, and how to standardize them. Our regular bloggers, Phil Garrou, Dean Freeman, Julia Goldstein, and Mark Berry; along with member guest bloggers, tackled the topic from their areas of expertise to create a **library of chiplet information**. You'll also find three new articles on chiplets on these pages: ***Chiplet Integration: Challenges and Solutions for Hybrid Bonding*** by Monita Pau, Onto Innovation; ***Excitement Over Chiplets: Not for Everyone and Not Trivial for Test***, by Mark Berry, Consultant; and ***Building a Chiplet Ecosystem*** by John Park, Cadence.

Sustainability; workforce development; and diversity, equity, and inclusion continue to be ongoing conversations that are critical for the growth of our industry. We are concerned about the impact aggressive industry growth targets will have on our natural resources; and where the workforce to support growth will come from.

Julia Goldstein's contribution to this issue, ***Has Our Industry Become More Sustainable?*** examines our industry's progress, and provides a scorecard of our member companies. In his Executive Viewpoint, ***Creating a Semiconductor Workforce for the Future,*** Dean Freeman addresses the challenges of getting students excited again about designing and manufacturing semiconductors. In **Hiring and Retaining a Diverse Workforce,** Robin Davis (Deca) and Jessica Grafeen (Textronix) provide some practical tips hiring managers can use. Both articles discuss the U.S. CHIPS and Science Act's role in workforce development.

For me, the best part of 2022 was the return of in-person events. There were so many I couldn't possibly cover them all myself! As Official Industry Partners of the International Microelectronics and Packaging Society, we participated in the Device Packaging Conference, the Advanced SiP Conference, and the International Symposium. We hosted our 3D InCites Awards at IMAPS DPC as well as our inaugural Hike for DEI, sponsored by KLA. We were also the official podcast for all these events. We participated in and podcasted from SEMI ISS, ECTC 2022, SEMICON West, and SEMICON Europa. Steffen Kröhnert represented us at SEMI Europe's 3D System Summit in Dresden, and ESTC 2022 in Sibiu, Romania. Our new test guru, Mark Berry, reported back from the IEEE ITC on the Chiplet UCIe. Dean Freeman attended IEDM on our behalf in December, and also provided reinforcements for SEMICON West. We captured memories from all these events in the **Year in Pictures**.

We hope you enjoy this Yearbook issue! We're already looking forward to what 2023 will bring.

Building a Chiplet Ecosystem

By John Park, Cadence

The semiconductor industry's decades-long adherence to Moore's Law doctrine of doubling transistor counts on monolithic devices every 18 – 24 months has been amazingly successful. It's now possible to integrate tens of billions of transistors onto a monolithic die whose area may be hundreds of square millimeters. The resulting chips provide massive amounts of horsepower for current applications such as high-performance computing, machine learning, graphics, and gaming; as well as for emerging opportunities such as implementing the metaverse.

However, the rising costs of designing and building chips on leading-edge processes limit access to the technology. Although the demand for functional integration continues to grow as more markets take up the advantages of electronics and system designs become more diverse, many applications cannot make an economic case for pure monolithic integration. Another way must be found to ensure that the considerable advantages of integration remain widely available.

IC packaging innovation tends to move hand-in-hand with IC process development. The latest step along this path is the development of 'chiplets': Bare dies that carry a particular function and have an electrical interface that enables them to be interconnected using silicon interposers and assembled into 3D systems-in-packages (SIPs) *(Figure 1)*.

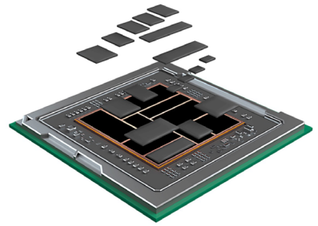


Figure 1: The chiplet concept disaggregates SoCs to make their functionality more widely available.

There are many advantages to this approach. The first is that it can create much greater functional densities than could be achieved using packaged chips connected with a PCB, or even package-on-package techniques. The second is that it enables designers to choose the right process for the functionality. Designing analog and mixed-signal circuitry that works consistently on leading-edge processes across all process corners is hard. This ability to match functionality to process can also lead to higher performance. Think of the advantages of putting RF circuitry on a high-frequency process rather than vanilla CMOS.

Perhaps the most intriguing opportunity of a shift to chiplet-based designs is that it could spur the development of a market for chiplets carrying standard functions, such as high-speed I/O or analog-to-digital converters. Designers could then assemble their choice of such chiplets to produce highly optimized 3D SIPs—achieving SoC-like integration and performance much more quickly and cost-effectively than would be possible by attempting the monolithic route—if that was even an economically viable option.

However, the development of a chiplet ecosystem comes with technical and business challenges *(Figure 2)*.

The technical challenges include managing thermal issues in such dense assemblies; ensuring the physical integrity and electrical performance of all the interconnect; dealing with the dramatic growth in the design space that a shift to using chiplets implies; verifying the resulting design in multiple ways; debugging, failure analysis, and more.

One of the key organizational challenges is managing the way that the use of chiplets blurs the line between IC design and PCB and package design. Each discipline will have to learn more about what the other does, and systems designers will have to understand it all, with access to tools and design flows that bring together aspects of interconnect, IC, and systems design strategies in a tractable way.

Other challenges arise for traditional package designers, including making the transition from understanding laminate-to-silicon-substrate layout and taking on the physical verification process required for silicon interposer designs. There are also electrical and thermal analysis challenges that must be addressed with tools that support in-design and electrothermal signoff, for on-chip and off-chip devices and interconnect.

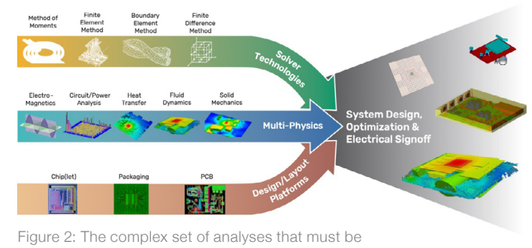


Figure 2: The complex set of analyses that must be applied to SIP design with chiplets.

IC designers making the move from monolithic devices to multi-chiplet architectures will have to learn how to plan, manage, and optimize their top-level design and connectivity. This will demand a new breed of tool that can aggregate data from the IC, package, and board design to enable system-level optimization and the development of the top-level netlist necessary for verifying correct connectivity (Figure 3).

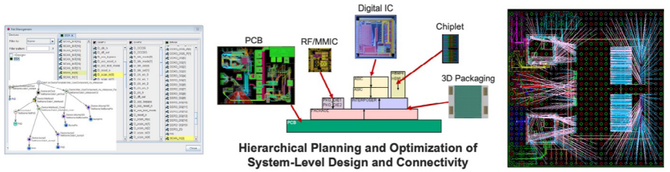


Figure 3: Hierarchical planning and optimization of system-level design and connectivity,

The business challenges of establishing a chiplet-based ecosystem may be as complex as the technical ones. When companies make monolithic SoCs, they rely on established test strategies, carried out in-house or by a partner, to ensure their products are working correctly. When their products become complex assemblies of chiplets from multiple vendors, assembled on an interposer made by another company and packaged by a third, the responsibility for final product testing, correct functionality, and overall yield becomes unclear. Many of these issues have been addressed in the development of MCMs, but the solutions, such as the use of known good die (KGD), will have to be retooled for the new level of complexity implied in 3D SIP designs.

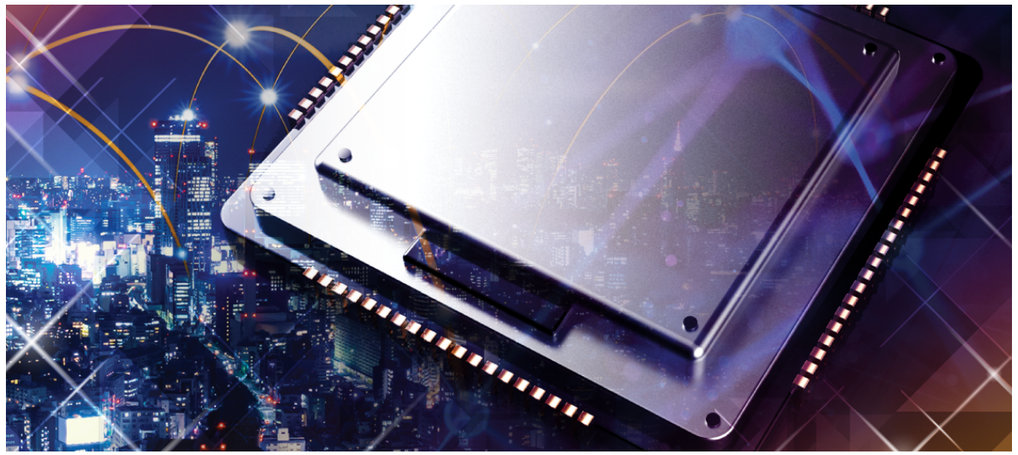
Interconnect will obviously be an important enabler for a chiplet-based ecosystem. Companies such as Cadence already have design IP for many forms of on-chip and off-chip interfaces, which customers can instantiate as standard I/O chiplets for use on multiple 3D-IC designs. This will enable them to match their manufacturing process choices to the needs of the I/O standard—for example, to enable them to instantiate electro-optical interfaces.

This design reuse proposition should appeal to large OEMs that can find such common functionality in their product roadmaps. What would make the chiplet ecosystem even more attractive is if such chiplets could be shared outside of a single company, thanks to a common interface standard.

The Universal Chipset Interconnect Express (UCIe™) standard is being developed to serve exactly this purpose, defining physical interface characteristics such as trace widths, bump pitch and channel reach, and electrical characteristics such as data rates and formats, latency, bandwidth, and testing and compliance issues.

If UCIe takes off, it should make leading-edge functionality available to designers who need to build highly integrated 3D-ICs but cannot make an economic case for monolithic integration on leading-edge processes. Chiplet-based design, though, still needs the support of tools that take a holistic view of the process, and IP that standardizes interconnects. Testing and debugging methodologies must also be improved to deal efficiently with multi-die scenarios.

If all this can come together, end customers can look forward to a continuation of the functional integration trend that Gordon Moore set the industry upon all those years ago.



Heterogeneous IC Packaging: Building an Infrastructure

By Mike Kelly, Amkor Technology, Inc.

Heterogeneous packaging is here. It is already in production, and increasingly more customers are developing and qualifying their products at Amkor and in other outsourced semiconductor assembly and test (OSAT) suppliers and foundry providers.

The rationale for this surge into new multi-die embodiments has been well documented and discussed. In the final analysis, more of the system content is moving into the package itself, with benefits in performance, cost, and time-to-market (TTM). Total silicon costs can be lower due to better yields for smaller chiplets. Heterogeneous packaging also provides the opportunity to use a mixture of silicon process nodes to further optimize the cost of the silicon. While heterogeneous IC packages are more expensive, the positive tradeoffs/benefits are lower total silicon cost and positive TTM benefits. Moving to a heterogeneous approach requires an infrastructure to be established in design, IC and package fabrication, and test.

IC packaging options to support chiplets and the heterogeneous constructions have propagated as each OSAT and foundry offers its own version. As a result, the terminology has become quite confusing. Thankfully, these package constructions are much simpler than the terminology that is now present in the industry. Multi-die products must be integrated into one functional unit and that is done on either classical IC package substrates or by using higher-density integration approaches, namely wafer-scale multi-die modules, ultra-fine line integrations, or both. The module is then attached to the IC package substrate.

The first option is typified by the long-standing multichip module (MCM), which has been in production for decades, with modern designs trending to higher silicon and passive density on the substrate. The second option for higher-density integration approaches is to create modules that integrate the die or chiplets, which needs ultra-fine-line routing for die-die interfaces. Today, these are (A) modules based on silicon interposers – 2.5D through silicon vias (TSVs), (B) modules based on high-density fan-out (HDFO) multi-layer redistribution layer (RDL) approaches, or (C) modules with bridges as shown in Figure 1.

Heterogeneous Packaging Designs

Modules based on HDFO interposers have been internally qualified, are customer products, and are in qualification. The quantity of different devices using HDFO interposers in the market is still

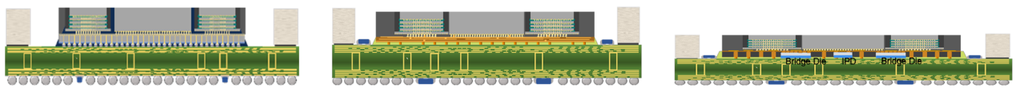


Figure 1: a) 2.5D TSV (silicon interposer, b) HDFO (S-SWIFT™) RDL interposer, c) Bridges (S-Connect) (RDL+ Bridge (s)).

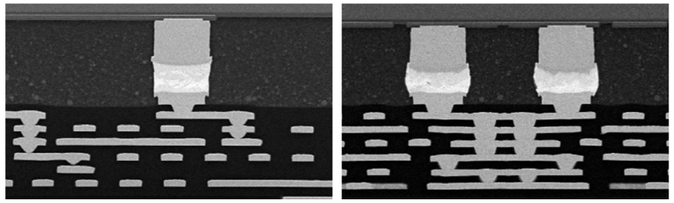


Figure 2a: Test vehicle die connected to HDFO.

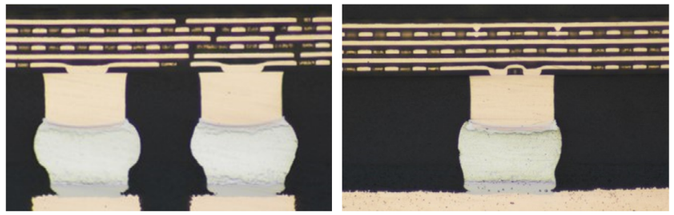


Figure 2b: Test vehicle HDFO module connected to package substrate.

limited as the transition to chiplets has just been initiated. However, the market is changing and most advanced packaging customers that are already producing higher-end monolithic or MCM devices are either actively qualifying HDFO interposers or inquiring, with the intent to start development.

In the initial planning phase of a product that incorporates an HDFO module, it is important to understand that each device is likely to be considered "custom." While the qualification envelope may encompass the overall module and package size under consideration, each device has unique challenges. For this reason, almost every new device has iterations of test vehicles (TVs). As more TVs are successfully completed and more of the possible design space variety is qualified, moving directly to product qualification will be likely, but for the moment, a TV is highly advised.

The first typically used TV is a daisy-chain die or at least bumped dummy die to allow for the discovery of any unique characteristics of the multi-die layout in the module. Assessing the interposer carrier and overmolding wafer-level warpage is a good example. Mechanical simulations can be used to estimate warpage but although simulating full wafer-level warpage is possible, it is also very sensitive to things like metal density in the RDLs.

It is always possible to establish trends in simulation, but the final assessment needs to be established with actual TVs. Since TVs can be internally fabricated relatively quickly, a simulation can be calibrated to real-world data quickly so that the trends can be understood when changing different elements in the model/device. By building the mechanical or daisy chain TV, data can be gathered quickly to understand where any engineering efforts will need to be focused. This has been repeated over many TV constructions to date and is a well-known process development path in Amkor. Figures 2a and b show typical TV approaches.

The second TV can be another daisy-chain device or have some minimal functionality or chip-package interaction (CPI) test structures in the die(s). Even though the dies are likely not fully functional, the design itself will either be similar to the functional design or can actually be the functional design. The design of the interposer RDLs typically starts before the first TV, since the chiplet interfaces are still customer-specific between dies. Finding the best routing strategy requires close collaboration between the customer and fabricator, as the design rules are continuously improving. Depending on when the product is targeted for production, more advanced design rules that are still in development may be available, which would enable routing that initial design rules would not allow. Every customer has their own preference for the design process flow. Amkor tries to accommodate all preferences, ranging from receiving only the finished graphic data stream (GDS) of the interposer to managing the entire design process.

The HDFO interposer design process typically begins with a starter database provided by the Amkor design team in either Cadence Calibre (SIP/MCM file) or Siemens Expedition. The starter database is not required but automatically initiates with the standard design rules and necessary settings to interface with a Calibre design rule checking (DRC) implementation, thus saving time. Amkor can also help to set up these parameters in whichever electronic design automation (EDA) tool is used. The Calibre DRC rule deck can be run either by Amkor or the customer since it runs directly on the GDS that is exported from the EDA tool.

For larger, more complicated interposers, the design process can range from 4 to 12 weeks. The EDA tools have improved significantly in the years since Amkor introduced its SWIFT® HDFO technology. The dynamic fill step can take significantly longer to process than most designers are accustomed to, so anticipating the added time in a production schedule is important at the outset. This is due to the extremely high number of pins, traces, and shapes present in the design. Degassing or thieving, depending on which is desired, is typically the last operation performed before the design is released. Amkor has developed approaches that can reduce the time degassing or thieving takes, but for large designs, this can be a multi-day activity.

Once the design is complete, it is released to the HDFO line to start the RDL build-up process. While the second TV's HDFO interposer is being fabricated, data will typically be collected on the first TV. This allows planning for any required design of experiments (DOEs) on the second TV. Not every device requires DOEs, but this is a crucial step so that any required improvements can be

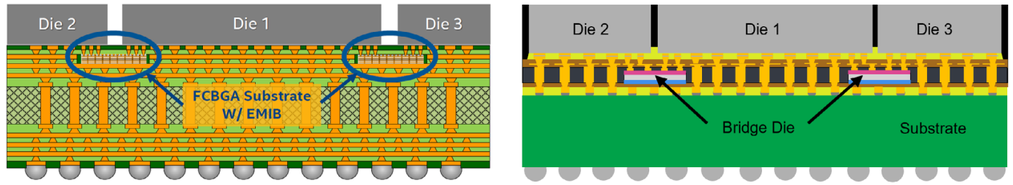


Figure 3: (L) Intel EMIB (Image courtesy of Intel) (R) Amkor S-Connect

flagged and either fixed or mitigated before the start of the assembly of the second TV.

The second test vehicle is typically used for package qualifications. HDFO modules have proven to be incredibly robust, passing moisture sensitivity testing level 1 (MSL1) and Temperature Cycle, Condition C (TCC) (-65°C to +150°C). Once attached to substrates, it is more common to evaluate at MSL 4 and Temp Cycle, Condition G (-40°C to +125°C), but success has also been achieved with the more stressful TCB (-55°C to 125°C) for > 3000 temperature cycles. Overall, HDFO has proven to be a very robust construction when it comes to package reliability.

The standard High-Temperature Storage (HTS) test (150°C, 1000 hrs) and standard Unbiased Highly Accelerated Stress Test (UHAST) for large body packages (110°C, 85% relative humidity (RH), 264 hrs) also have seen no issues in package qualification. In most cases the second TV uses the functional HDFO interposer design, so once the package qualification is complete, it is ready for the functional silicon qualification.

The industry has been working on methods that utilize bridging technologies for several years. Intel's embedded multi-die interconnect bridge (EMIB) utilizes a bridge placed within the organic substrate to allow high-density routing without the use of silicon interposers. Amkor's approach to this space embeds a bridge (silicon or other) into an HDFO design and this brings ultra-high-density design rules to the HDFO toolbox. Amkor refers to this technology as S-Connect. Figure 3 shows a comparison of these two design techniques.

When working with customers and industry partners the decision between silicon interposer, organic RDL HDFO, and bridge solutions like S-Connect, requires a trade-off analysis. The decision to go with bridges must address sourcing of the bridge die (with or without TSVs) and the silicon-integrated passive device (if warranted). The overall production readiness and maturity

of each solution are also considered by the end customers. Silicon interposers are the most mature, as they have been in high volume manufacturing (HVM) for many years, followed by organic RDL with many successful qualifications complete and S-Connect, respectively. As systems become more complex, the need for integration may force solutions toward a bridge solution such as S-Connect.

There are three primary drivers for bridge technology. Bridge technology allows a reduced number of RDLs through the inclusion of silicon-based, high-density routing bridges for chiplet-to-chiplet or die-to-die routing, which in turn can lead to the potential for reduced system cost. Bridge technology also makes use of fab lithography that permits routing densities below 1 µm, which can facilitate finer bump pitch on the silicon top die. Finally, the use of the bridge technology allows for the creative use of embedded silicon integrated passive devices (IPD) in the same 3D location (see Figure 4), placed directly under the top die for optimal power delivery.

HDFO design and fabrication are available in die-first or die-last configurations. For simpler and smaller designs, die-first may be appropriate and a somewhat lower-cost approach. Amkor's primary path for S-Connect designs uses a die-last approach to leverage expertise in die-last HDFO technology and to minimize the yield impact on customer silicon.

Die-last S-Connect construction is composed of a base RDL with preformed tall copper pillars. The bridge die and other non-bridge dies (including IPDs) are placed face-up with smaller copper pillars. The wafer is molded and planarized to reveal all the copper pillars. Die placement capability is a crucial process requirement, which becomes more complex as the number of face-up bridge dies are placed in any given product. Additional RDL processing is then performed using an organic RLD process like HDFO with a die attach pad provided for die attachment. Chip-on-wafer assembly is then completed with a second mold and mold grind process. The wafer is then removed from the carrier and flipped over for back-side processing, where controlled collapse chip connection (C4) copper pillars are plated. At this point, the module formation is completed, and it fits into a common process used for other integrated modules.

Bridge die sourcing is another key aspect when contemplating S-Connect over other forms of heterogeneous integration. Customers may require the bridge to also have TSVs to provide power and ground into the I/O PHY. Sourcing and processing of these TSV-bearing bridge die will make the wafer-level fabrication of the S-Connect module more complex. Amkor has significant TSV process experience including a vast set of chemical-mechanical planarization (CMP)/backside passivation recipes to choose from that should minimize the development needed in the preparation of the TSV bearing bridge.

Presently, there are two internal TVs for S-Connect development. Development and internal qualification have been completed on three die modules comprising a larger die and two smaller (like high bandwidth memory (HBM)) die. The module has two bridge die and several test dies to mimic the placement of non-TSV bearing IPD die. On a larger scale, module TV development is occurring with 10 top die and 10 bridge die. This demonstration targets the very large modules, which benefit most from the use of silicon bridge die. Reliability results are expected on this TV in 2023. Figure 4 shows the two S-Connect test vehicles.

Amkor has been preparing for this next evolution of heterogeneous integration and we believe it will provide unique capabilities to augment the HDFO and silicon interposer solutions as more integration is required. With larger interposers (>2500 mm^2), bridge solutions will help keep yields high as the highest density requirements (and highest potential yield loss) are on the bridge, which already has an extremely high yield.

Test

Amkor has been offering test services for heterogeneously integrated products since the beginning of these designs. The systemic approach of designing and evaluating the TV allows the test engineers to develop tests for critical aspects of the design before the live product.

There are a handful of test challenges that are common to all heterogeneous chiplet packages. Chiplet interconnect integrity is an important one. Signal and power delivery to every chiplet within the package requires careful layout, design, and test during the manufacturing process. The package material type impacts the interconnect performance between the chiplets and to the pins exposed at the package level. This includes both static connection quality with continuity, leakage and transient ac timing, impedance matching, and signal crosstalk. In a carefully designed overall product architecture, design for test (DFT) access to all functional aspects of the product is an important consideration.

IEEE1838["IEEE Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits," in IEEE Std 1838-2019, vol., no., pp.1-73, 13 March 2020, doi: 10.1109/IEEESTD.2020.9036129.] is one such standard that helps during the architecture phase of the product. The thermal performance of each chiplet also impacts production testing. Thermal gradients due to non-uniform chiplet temperatures are common. A controlled, managed and repeatable production test environment ensures accurate feedback for future product design iterations and consistent yields.

Conclusions

Heterogeneous integrations using MCMs and the venerable 2.5D TSV silicon interposer approach have been in production for years. The transition to heterogeneous chiplet-based integrations is just beginning.

To integrate chiplets, a typical design must have a high-bandwidth interface between the die, and this normally necessitates fine bump pitches (≤55 µm), high signal rates, and short bus lengths. HDFO and S-Connect designs provide a cost-effective path for these integrations. Typical designs are less than 2500 mm2 but the trend is currently strong toward larger sizes and higher die counts.

For larger modules, the use of bridges makes sense. Large modules (>2500 mm^2) using very fine-line RDL will cost more due to RDL yields. Using extremely high-yielding bridges to provide the finest routing between die, combined with lower density RDL elsewhere, will be a better economic tradeoff due to higher expected total yields. The bridge packaging solution is being developed and is targeted for customer qualifications in 2023 and 2024. HDFO chiplet integrations have been internally qualified and HDFO is ready for customer engagements and product qualifications. Best-in-class test services for heterogeneously integrated products complete the manufacturing process.

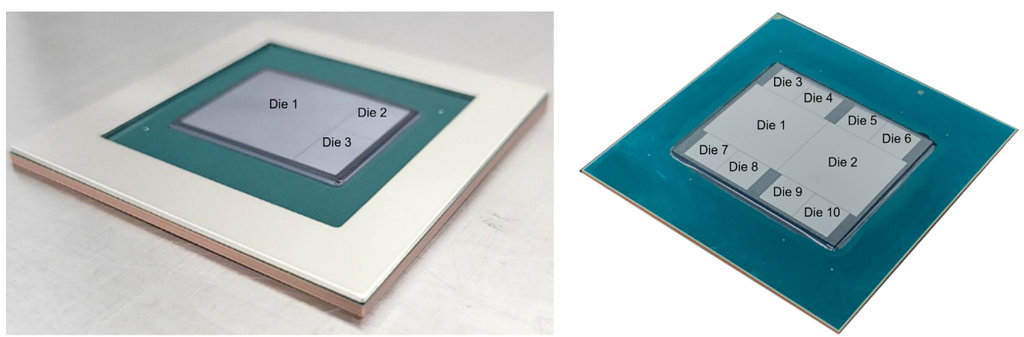


Figure 4: The types of S-Connect test vehicles.

Please contact Mike Kelly at **mike.kelly@amkor.com** to discuss any of the options discussed above.

The Rise of Organic and Glass Substrates

By Keith Felton, Siemens EDA

If you are designing a heterogeneously integrated, multi-die, high-performance device for markets such as HPC, AI, data centers, etc., then the silicon interposer is probably the platform of choice. Yes, it comes at a cost, and generally requires expensive silicon place-and-route (P&R) tools, along with workflows for implementation. With the emergence of new organic and glass substrates, and advanced IC packaging design solutions, this is all starting to change.

There has always been a drive to find more cost-effective solutions for silicon interposers that can still deliver the required performance. Intel pioneered this path with its embedded multi-die interconnect bridge (EMIB), which allowed the use of low-cost, proven, organic materials for the overall substrate. Soon most OSATs and substrate suppliers had their own version of EMIB. While cheaper overall, it still involves a complex substrate assembly process.

Several companies, such as Absolics, have been exploring glass as a high-performance, yet low-cost platform. This technology is showing great promise and is expected to see increased adoption as we go into 2023 and beyond. Glass substrate-based designs offer low loss and very high data transfer speeds while offering lower power consumption and thermal stability. The design methodology workflow for glass is very similar to advanced organic interposers such as RDL build-up, made popular with TSMC's 3DFabric's Integrated Fanout (InFO) technology as well as similar solutions such as ASE's FOCoS and Amkor's SWIFT.

With glass interposers ideally suited for HPC, AI, etc., the subsequent designs are considerably challenging and require the design tools and workflow to support multiple capabilities not typically required for conventional laminate core packaging *(Figure 1)*. This is where advanced semiconductor packaging design solutions triumph as they deliver all the capacity, performance, and capabilities needed without traditional expensive and Linux-limited P&R limitations, given that most semiconductor heterogeneous integration is the responsibility of packaging design teams.

The first area designers of advanced organic and glass substrate-based designs need to focus on is planning and prototyping; not just of the base substrate but the entire package assembly. Planning and prototyping the entire package assembly holistically using system-technology co-optimization (STCO) techniques results in a completely optimized digital twin model of the design *(Figure 2)*.

During design planning, the designer must use predictive analysis to ensure that the chosen design scenario can achieve routing, signal, power, and thermal requirements. Predictive analysis is not a detailed analysis. At the planning stage the design is just a prototype, lacking the 100% fidelity of a completed design, so predictive analysis is not sign-off accurate. Instead, it's fast allowing for rapid tradeoff decision-making that helps the package design architect refine the prototype and arrive at the ideal implementation scenario. Now given the typical application focus of advanced organic and glass interposers the resulting designs are going to be very large with extremely high pin counts and expansive connectivity structures. Therefore, the capacity and interactive performance of your implementation design tools should be one of the first things you consider.

The next area is high bandwidth memory (HBM) channel design support. Ideally, the design methodology should have a high degree of automation to ensure productivity and reduce potential errors so often introduced when using manual design methods or tools without sufficient rule support and HBM channel replication. Because such designs are large, complex, and dense, the need to design concurrently with multiple designers working in parallel is commonly seen as a prerequisite for success. Leveraging multiple designers with different areas of expertise is further enhanced if the concurrent design can be achieved across geographic borders.

The next area of focus is around multiple fabrication and manufacturing requirements such as advanced metal layer balancing and degassing. This is another challenge that must be addressed in tandem with the creation of complex power and ground structures that need to provide sufficient power delivery without unacceptable levels of IR drop. These designs can often benefit from reusing known good design IP within and across designs to speed implementation and reduce risk.

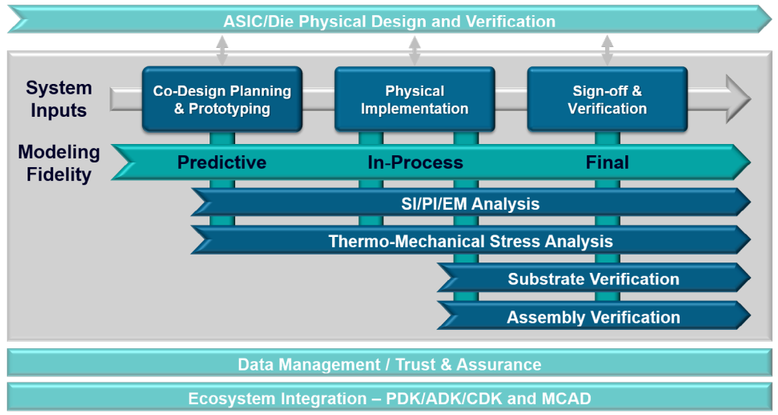


Figure 1: Siemens interposer package design with workflow.

These advanced designs benefit from design tools and design workflow automation and customization, such as the ability to easily develop custom substrate-specific design rule checks (DRC) that can be used during design. Of course, even when the design is complete it needs to undergo rigorous substrate and assembly connectivity (LVS) verification using the actual manufacturing data, typically GDSII or OASIS, why? Because you need to verify the actual data that will drive fabrication and assembly/test. Performing detailed DRC during design is important but it's not signoff. Using the actual manufacturing data is signoff.

In summary, it's clear that 2023 will see further advances in our quest to get more from Moore with new organic and glass substrate technologies and platforms, as well as advanced semiconductor packaging EDA design solutions.

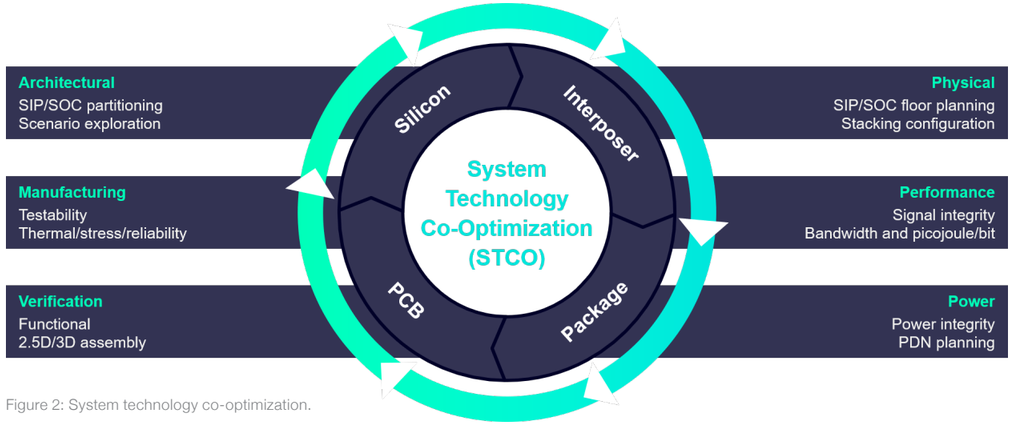


Figure 2: System technology co-optimization.

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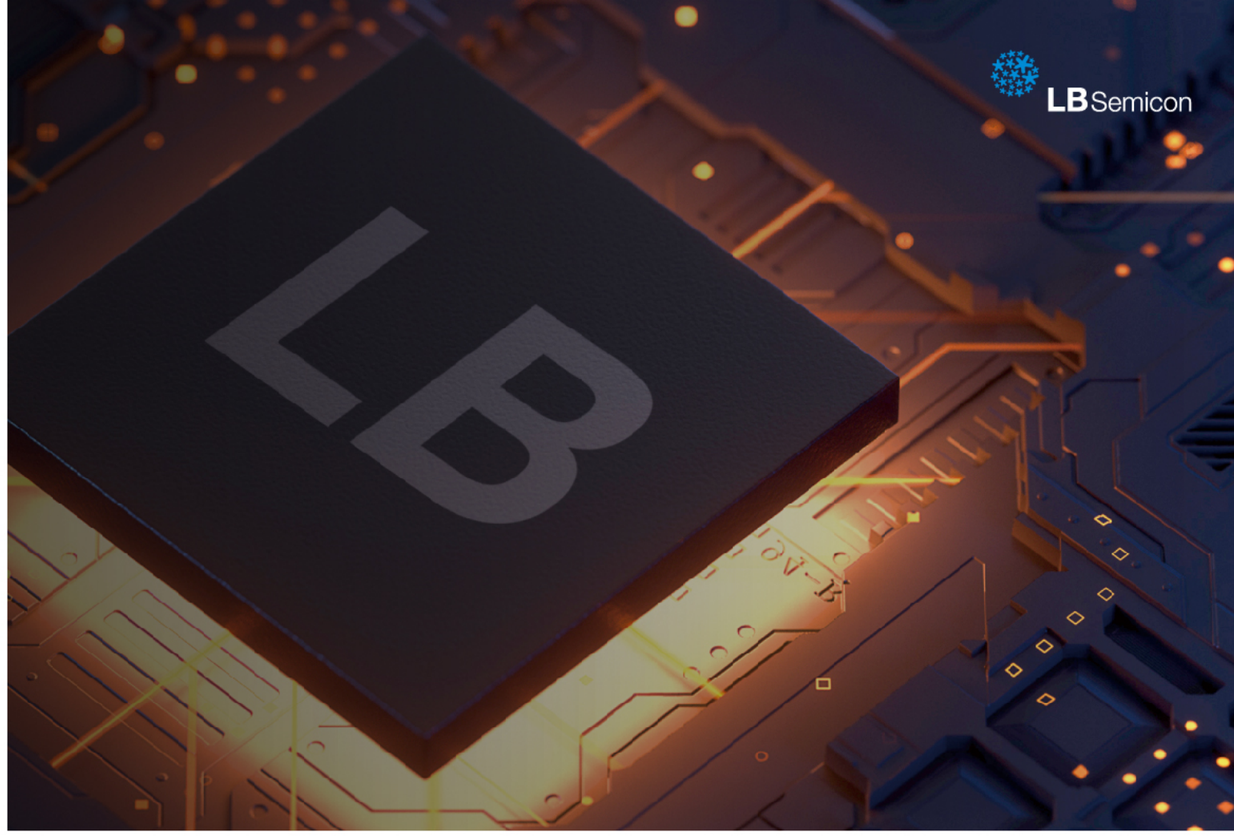

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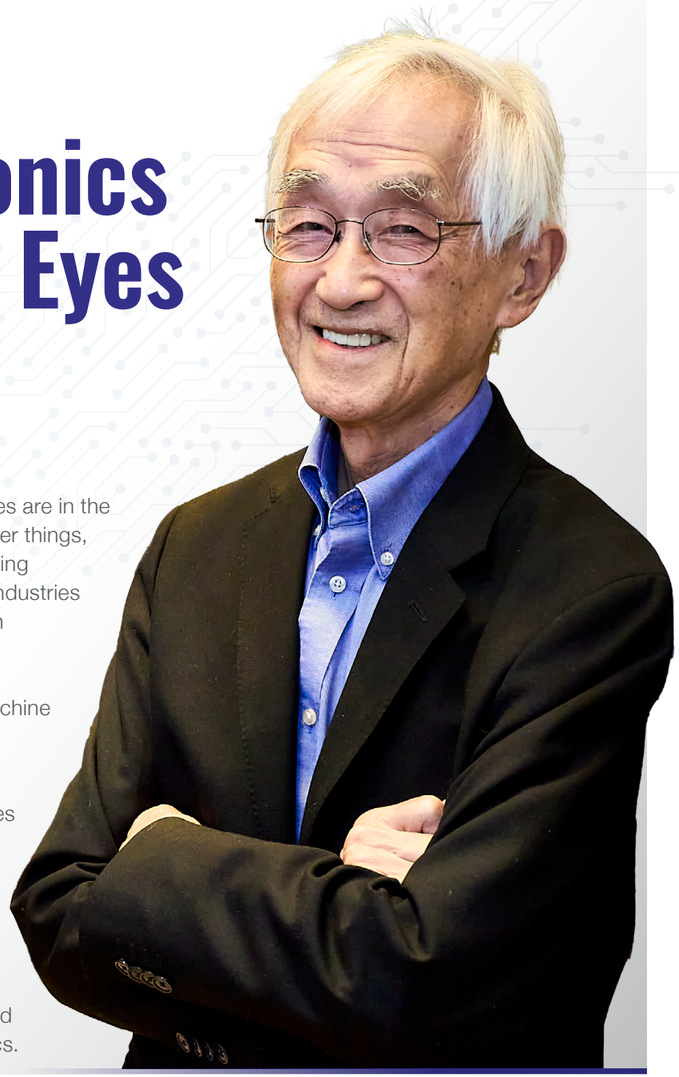
A Career in Microelectronics Through the Eyes of Bill Chen



By Françoise von Trapp

The semiconductor and microelectronics industries are in the midst of a workforce crisis created by, among other things, the combination of explosive growth and a maturing workforce. Competition for STEM talent in other industries has made it difficult to recruit the latest generation of graduates, who are lured by seemingly sexier opportunities in the end-use application space at companies implementing artificial intelligence, machine learning, augmented and virtual reality, and more.

It wasn't long ago that semiconductors and microelectronics provided the sexiest opportunities for engineering graduates. Back in the 1960s, that's where all the exciting developments were happening. And without that early work, we wouldn't be where we are today. Ask anyone who works in the industry and they'll tell you that it's still an exciting place to work today because none of the "cool" devices we use every day would exist without semiconductors and microelectronics.

For this cover story in the 2023 Yearbook, I decided to talk to an industry veteran whose engineering career evolved in lockstep with the microelectronics industry itself, in hopes of inspiring the latest generation of talent to pursue careers in these critical, foundational, and exciting industries.

In 2022, William (Bill) Chen ASE Fellow and Senior Technical Advisor at ASE Group, was awarded The Daniel C. Hughes, Jr. Memorial Award by the International Microelectronics and Packaging Society (IMAPS) for his technical achievements related to microelectronics, combined with outstanding contributions supporting the microelectronics industry, academic achievement, or support and service to IMAPS. I asked him to share his microelectronics journey with us.

Recalling the Early Days

Talking to Bill Chen about his career in microelectronics is like jumping into the pages of a history book. After six decades in the industry, Bill has seen it all, and ridden wave after wave since completing his Ph.D. work at Cornell University, and joining the IBM Development Laboratory in Endicott New York in September of 1963. Endicott was IBM's birthplace and was the original manufacturing site for computer systems, high-speed printers, and electronic components. That was pre-Moore's law.

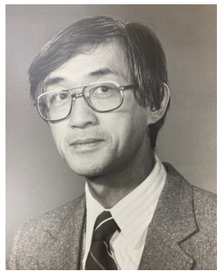
"At that time, both the microelectronic and computer industries were much smaller than they are today," Bill recalls, "But they were already both recognized as an important part of the global economy."

Back then, computers were large, bulky, and expensive. They were owned and operated mostly by large financial and governmental institutions. The consumer electronics revolution was yet to happen. People understood that computing advancement was facilitated by innovations in science and technology based on semiconductors and microelectronics.

"While it was a long time ago, it does seem like yesterday," said Bill.

Choosing His Path

As a newly newly-minted Ph.D. doing his postgraduate course in science and engineering at IBM product development and problem-solving, Bill joined the Advanced Mathematical Science group. The team comprised people with different backgrounds, experiences, and interests.



"I was an engineer interested in addressing problems in microelectronics. It was a fast-moving field in a fast-moving industry," Bill explains. "When I joined IBM, I look around to see where my engineering knowledge could be applied and learned how to work together with people from other disciplines and backgrounds. I learned to be creative in addressing engineering issues, posing questions, and how to build on knowledge and intuition."

Bill also learned that one of the most important things to understand in product development was the product's design life. This involved knowing which components were most critical, how to test a product design's robustness, and when sufficient data would be available to confidently launch the product.

"I started to think about how to apply my knowledge to these issues, which lead to a path in engineering," he said. "I was interested in predictive modeling that starts early in the design phase to understand how things work, how they fail, and how to make them robust enough to last."

Microelectronics research has been at the core of Bill's career. While he was at IBM, the company was deeply involved in research and development in everything to do with computers, from integrated circuits to ceramic packaging and printed circuit boards. He found his niche in electronics packaging technologies, supported research across IBM's global sites, and volunteered at universities.

When the National Technology Roadmap for Semiconductors (NTRS) was first organized, Bill participated in its working groups, as well as when it evolved into the International Technology Roadmap for Semiconductors (ITRS). In 2016, as semiconductor technology appeared to reach its scaling limits, the ITRS published its last edition. As it became clear that the path for continuing along Moore's Law was in heterogeneous integration through advanced packaging technologies, Bill, along with colleague Bill Bottoms, spearheaded the Heterogeneous Integration Roadmap (HIR), which published its first edition in 2019.

"I am very glad that these humble beginning has helped me to contribute to society over the years," says Bill. "At ASE, my role consists of very little hands-on engineering work and has shifted to being strategic, connecting, advisory, and mentoring. There is great satisfaction in seeing the teams grow in knowledge, strength, and stature, and to see individual engineers and technologists rising to difficult challenges to our complex and expanding electronics industry."

Being Part of the Advanced Packaging Evolution

For someone like me, who entered the industry in 2005, the term "advanced packaging" has always been part of the microelectronics lexicon. So I found Bill's perspective enlightening because it extends back to the origins of advanced packaging. He remembers when the shift from gold to copper wire bonding was considered advanced packaging.

"I was fortunate to be involved when ASE led the industry in copper wire bond development, helping to solve the mysteries of copper wire materials, bonding equipment, and bonding processes," said Bill. "Now that a sufficient knowledge base and data have been built into industry specifications and test standards, wire bonding is used to package 70-80% of the global semiconductor components. But it is no longer considered advanced packaging."

Bill explained that like most engineering technologies, packaging technologies have evolved with innovations in materials and equipment developments, as well as in design and architecture. For example, fan-out (FO) technology started with the reconstitution process to address wafer-level chip-scale packaging (WLCSP) components that had insufficient silicon real estate to accommodate required I/O solder balls. Since then, FO technologies have evolved into high-density versions that address multiple-chip integration. It is a highly versatile packaging technology used in leading-edge applications.

"We are still in the early stage of this technology development," notes Bill. "There will be innovations in design, materials, and assembly equipment as semiconductors move into lower and lower digit nodes and electronics system requirements continue to

broaden." He predicts that FO technology will share the high-performance applications stage with silicon interposers in high-performance computing.

Fan-out is just one part of the heterogeneous integration offering that Bill says is leading to complex packaging integrating multiple chips into a single package, including system-in-package (SiP) and chiplets.

"With heterogeneous integration, innovations across our whole industry is broadening from high-performance computing, data centers and networks to automotive, smart phones, aerospace and defense, medical and health, IoT and the edge," notes Bill. "At one time the industry was focused on pacing to the next node. Now the market and application spaces are broader and more diverse. The world of heterogeneous integration will be rich with creativity and innovations. The important part for all of us is to bring the whole ecosystem along for the ride."

Highlights, and A-Ha! Moments

It's not easy to look back over a career that helped a fledgling industry become a global powerhouse and select just a few highlights. For Bill, one of the earliest highlights was gaining recognition for his early work at IBM in predictive modeling, using simulation and modeling verified by experimental design. This proved to be useful in product design from the early conceptual stage to manufacturing.

"The semiconductor industry is exciting and I feel fortunate to have built up knowledge over the decades working throughout dynamic innovation and application cycles."

"While I was very pleased to receive an IBM Division President Award in recognition for my work, it was just as important to hear from a product manager or reliability engineer that the product went through qualification and production smoothly with few technology hiccups," says Bill.

Fast forwarding a decade or so, Bill says another career highlight, this time when he was at ASE, was working on an eight-year joint development project with AMD to develop and bring to market the first silicon interposer technology.

"While I did very little hands-on engineering work, my role being strategic, advisory, and mentoring, there was great satisfaction in seeing the team and individual engineers rising to the challenges to bring the project to successful fruition," he recalls.

Most recently, overseeing the HIR initiative has become another career highlight. "This was a collaborative project with many volunteers coming together with a common goal," He said. "It was truly gratifying to have the HIR released on October 10th, 2019."

I asked Bill what he tells his grandchildren when they ask about his career. Here's what he said: "I tell them that what I do is to gain knowledge, and build on the knowledge of many other people before me. And then I endeavor to do good with the whole body of knowledge. The semiconductor industry is exciting and I feel fortunate to have built up knowledge over the decades working throughout dynamic innovation and application cycles.

Advice to Industry Newcomers

There is no doubt that the world is much more complicated today than it was when Bill first began his career.

"When I started, the microelectronics world and its technology supply chain were much simpler," he says. "In those days when I had a technical issue that I did not understand it was possible to walk down the corridor to seek out someone and say. 'tell me what you know,' and then together walk down to another office and say, 'Tell me what we should do,' and then three of us together would collaborate to get the whole technical story together and solution in place."

Today explains Bill, it's much more difficult because in the worlds of microelectronics and semiconductors, the technology and supply chain knowledge is much more complicated. "One of the difficulties we have is finding people who understand not just the big picture, but its many detailed parts. That, I think, will be the big challenge," he said.

Hindsight is 2020

No career is without its challenges. Bill credits his early years at IBM with teaching him how a company works and how all the parts come together. There, he learned how to navigate the inter-company politics that come with working at a large company with a global footprint.

Would he do anything differently?

"Hindsight is 2020," says Bill. "2022 marked the 75th anniversary of the discovery of the transistor effect. 75 years is a very short time in human history. I am very fortunate to be in this profession at a time when the transistor, semiconductors, and electronics burst into the world. I appreciate the many people who helped me along the way and the many people who had faith in what I do. I cannot thank them enough."

Bill sees the growing complexities of microelectronics not as a negative, but as an opportunity. He's excited about the new era of heterogeneous integration. "I'm looking forward to the next decade of advanced packaging, years of heterogeneous integration, years of new devices, new industries, and new knowledge to learn," he said.

With his finger firmly on the pulse of heterogeneous ntegration, Bill exudes optimism and passion about the transformative innovation ahead. What could be more inspirational than that?

The Age of Hybrid Bonding: Where We Are and Where We're Going

By Monita Pau, Onto Innovation

For decades, Moore's Law has been a way to measure performance gains in the semiconductor industry, but the ability to double the density of transistors on a chip every two years is becoming increasingly challenging. With scaling reaching its limit, manufacturers are looking to advanced packaging innovations to extend the performance gains that the industry, and the world at large, have grown to depend on.
Cu-to-Cu hybrid bonding is one way the industry is looking to extend ever-increasing I/O density and faster connections, all while using less energy.

Primarily used in CMOS image sensor (CIS) devices today, hybrid bonding is poised to be the successor to microbumps in devices requiring high-bandwidth data transfer, particularly those designed for artificial intelligence (AI), high-performance computing (HPC) and graphics processor units (GPUs). However, microbumps are increasingly problematic at pitches under 10µm. A very small non-uniformity in the plated microbump height or variation in the solder reflow process may be negligible when the bump structures are large, but with fine-pitch microbumps, these small variations can lead to bad joint formation and affect the electrical yield. The end result: defective dice and packages.

Another challenge for scaling microbumps is that at such fine pitches, the solder of the bump may bridge, causing shorts. In addition, controlling the plating uniformity of these small structures is challenging, while the ability to find new, more suitable underfill materials to fill the shrinking space between the microbumps is also required.

The direct, fine-pitch Cu-to-Cu interconnects enabled by hybrid bonding will allow for 1,000 times the number of connections as microbumps. But as with all innovations, hybrid bonding poses challenges even as it enables higher-performance AI, HPC, GPU, and image sensors. Surface cleanliness, for one, is paramount.

A less-than-1µm particle on the bonding surface of an interconnect with a pitch that is less than 10µm will likely create a void in the bonded structure and impact the yield of the final device. However, on an interconnect of greater size and pitch, a 1µm particle would have a negligible impact on the process yield. For these reasons, advanced packaging facilities must use clean room standards approaching the front-end fab level, along with inspection tools to discover sub-micron particles and defects.

Other areas of concern include the warpage of the thinned wafer, alignment errors of the bonding surfaces, precise control of Cu pad height, and the generation of the divot-like gap that is filled by the bonding of the two Cu pads through thermal expansion. As such, high-performance metrology tools must be used as well.

In this article, we will discuss the trends leading to hybrid bonding, the challenges facing hybrid bonding, and the tools that provide the best solutions.

Why Hybrid Bonding?

The reasons for the transition to hybrid bonding, as opposed to microbumps, are fairly straightforward. 3D memory stacks and heterogeneous integration — two players in the More than Moore era — require extremely high-interconnect density. This is a need for which hybrid bonding can deliver. Compared to micro-bumping, which itself supports a high-density interconnect scheme, hybrid bonding delivers smaller dimension I/O terminals and reduced pitch interconnects. The standoff distance between each die is dependent on the height of the microbump, but this distance is nearly zero with hybrid bonding. As a result, hybrid bonding interconnect schemes can reduce the overall package thickness considerably, perhaps even as high as hundreds of microns in multi-die stack packages.

There are currently three approaches to hybrid bonding: wafer-to-wafer (W2W), one-by-one die-to-wafer (D2W), and collective D2W. With W2W bonding, two wafers are directly bonded to each other. This is a common method for backside illumination technology (BSI) architectures for CIS. With one-by-one D2W bonding, the die transfer uses a flip-chip bonder from a carrier to a destination wafer. With collective D2W, the dice are attached to a carrier wafer leading to the W2W bonding of reconstructed and destination wafers.

Today, hybrid bonding has been proven to be feasible in the high-volume manufacturing of 3D NAND stacks and 3D systems on a chip (SoC). Research and development are ongoing regarding the application of hybrid bonding in high-bandwidth memory (HBM), as well as other 3D integration applications when microbump pitch is less than 10µm.

The Market

From 2021 to 2027, the high-end packaging market is expected to grow by a CAGR of 22% based on the production wafer volume forecast from the Yole Group. These high-end applications include 3D NAND, 3D SoC, HBM, and 3DS, Si interposer/bridge integration, and ultra-high-density fan-out packages.

The adoption of hybrid bonding is at various phases for these high-end applications. Currently, 3D memory stacks are a volume driver for hybrid bonding and should remain that way, while 3D NAND is initially being adopted, a move that should be followed by HBM. In addition, the initial 3D SoC products that will use is unclear. We expect to see the rollout of more devices utilizing hybrid bonding in the next two to three years.

Challenges and the Process Control Needs

Although the performance-gain promises of hybrid bonding are all but certain to lead to the increased use of the bonding technique in the market, especially in high-performance computing, data center networking l and autonomous vehicles, the challenges posed by this emerging technology are significant to both assembly and testing. Overlay errors and yield-killing void defects are heightened problems, while electromigration, delamination, and copper diffusion greatly impact reliability. *(Figure 1)*

Not surprisingly, one of the more significant challenges at the pre-bonding step of hybrid bonding involves the interconnection of the two Cu pads that are to be joined. For the process to work and for the two pads to be successfully bonded, chemical mechanical planarization (CMP) must be used to ensure that the Cu pads have a suitably small surface recess into the oxide. This allows the two Cu pads to expand and touch, and eventually bond through the annealing process, while not unzipping the previously formed dielectric-dielectric bond around the Cu pads.

With all of this in mind, establishing and maintaining tightly controlled electroplating and CMP processes is necessary. Without such stringent controls, the bonding will not succeed and HVM will not be feasible. To accomplish this, high-precision, high-throughput metrology measurement, and control techniques are required to monitor the dielectric film and Cu thickness, as well as surface topography.

Particle control is a mandatory yet difficult part of the hybrid bonding process because so many back-end processes are prone to generating debris. These back-end processes include wafer grinding, wafer-edge trimming, wafer sawing, and taping/de-taping. While traditional back-end inspection requires defect sensitivity greater than 5µm, hybrid bonding requires a surface defect detection that is significantly less. Tools designed to meet the standards of hybrid bonding defect detection must have greater resolution and speed to detect these nanoscopic defects. Once the two Cu pads are bonded, failing to identify the critical size particles significantly increases the probability of creating voids 10 times or larger than the initial sub-micron particle.

During the hybrid bonding process, several key process steps bring different challenges and obstacles. In addition to the problem with particles and surface topography after CMP, other challenges include die cracks and wafer warpage. The post-CMP total thickness variation of the dielectric film across the wafer can also affect the bonding process. As a result, back-end fabs will need metrology tools for film thickness measurement, in addition to high-throughput inspection tools for die-level crack/particle detection.

Lastly, in the post-bonding stage, both inspection and metrology tools continue to play a crucial role in process control. These tools will need to measure bond line thickness and pad alignment and be able to identify voids. A high-speed infrared inspection system will be useful in identifying voids and other defects, but there are limitations when applied to identifying voids under metal.

Only known good die will be subject to hybrid bonding, and in the case of multi-die stacked 3D packages, such as HBM, this process must be repeated multiple times. Given the complexity and stringent requirements, tight process control is critical along each step of the stacking process. Analytics software capable of tracing the genealogy of each die and each process step can bring invaluable information for yield enhancement.

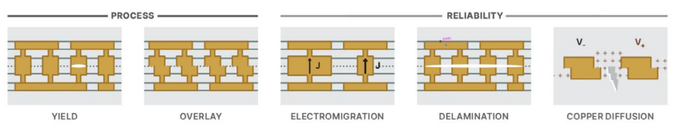


Figure 1: Heightened problems for hybrid bonding.

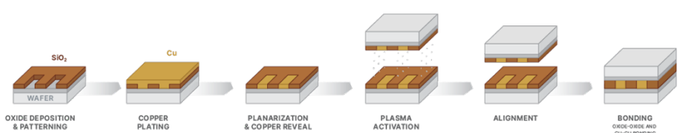
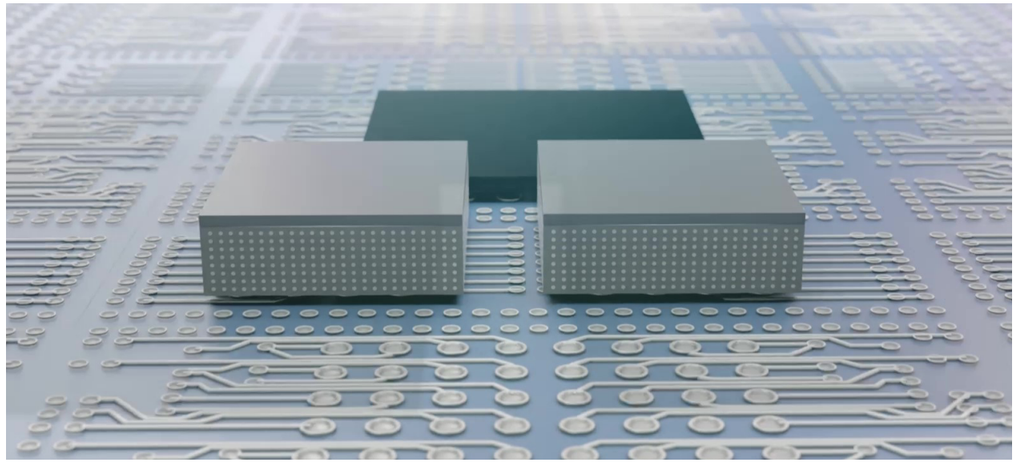


Figure 2: The hybrid bonding process.

Conclusion

The use of Cu-to-Cu hybrid bonding is moving beyond CIS devices as it is adopted for 3D NAND and 3D SoC. Even more applications are on the horizon. But this potential building block of the More than Moore era has significant challenges. For hybrid bonding to be successfully implemented, a wide range of tools is needed. Metrology tools can be used to measure pre- and post-CMP dielectric, Cu film thickness, and topography, as well as identify metal film stack voids. Inspection tools can be used to detect particles, cracks, and voids, whereas tools with infrared capabilities may have an advantage. Inspection tools can also be used to measure residual Si thickness and inspect the backside after thinning. Last but not least, analytics software can also be employed to enable chiplet and process traceability.

With these solutions and processes in place, hybrid bonding should see further and, possibly, rapid implementation, bringing with it performance gains to servers and networking switches, AI/ML and AR/VR, and autonomous vehicles.



Heterogenous Integration Moves to Another Level Using Hybrid Bonding

By Stephen Hiebert, KLA Corporation

Introduction

Part of the fun of playing with building blocks is the seemingly unlimited ways that one can put them together. Imagine adopting this concept to the semiconductor industry where you can take different kinds of chips and combine them like blocks to build something unique. Start with defined goals for performance, size, power consumption, and cost for your semiconductor product, then aim to meet the requirements by combining different types of chips into a single package. This concept of the heterogeneous integration of chips is already driving innovation across packaging technologies *(Figure 1)*.

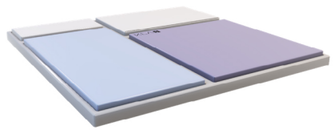


Figure 1: Heterogeneous integration combines different kinds of chips into one package

The adoption of heterogeneous integration in packaging has been accelerating recently to meet the increasing need for more complex functionality and lower power consumption. Heterogeneous integration allows IC manufacturers to stack and integrate more silicon devices in a single package. This can include the combining of chips from different wafers, from different semiconductor technologies, and from different suppliers. Heterogeneous integration also enables chiplet integration to overcome yield challenges for large die, as well as reticle size limitations.

As 2.5D, 3D, and fan-out packaging technologies have evolved, copper microbumps have provided the required vertical metal device-to-device interconnections into a single, integrated product. Copper microbumps, typically 40µm in pitch (25µm bump size, 15µm spacing), have scaled down to 20µm and 10µm pitch to increase package density and functionality. Below 10µm bonding pitch, however, microbumps begin to run into yield and reliability challenges. So, while traditional copper microbumps will continue to be used, new technologies are also being developed to continue increasing interconnect density. Hybrid bonding technology is emerging as a viable pathway for high-end heterogeneous integration applications where the interconnect pitch is 10µm and below.

Hybrid bonding enables an assortment of possible chip architectures, mainly targeted at high-end applications including high-performance computing (HPC), artificial intelligence (AI), servers and data centers. As the technology matures, further growth is projected into consumer applications, the memory including high bandwidth memory (HBM), and mobile and automotive applications that could benefit from the high-performance die-to-die connections.

What is Hybrid Bonding?

Hybrid bonding is a process to create a permanent bond between heterogeneous or homogeneous die. “Hybrid” refers to the fact that both dielectric-to-dielectric and metal-to-metal bonds are formed between the two surfaces. The use of tiny copper pads embedded closely together in dielectric delivers up to

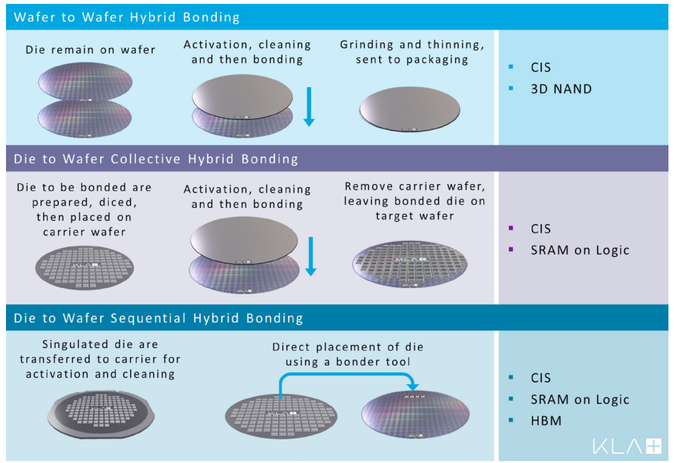


Figure 2: W2W and D2W hybrid bonding techniques and applications

1,000X more I/O connections than is possible with copper microbumps and is driving signal delay to near zero levels. Further advantages include expanded bandwidth, higher memory density, and increased power and speed efficiencies.

Hybrid Bonding Technologies

The key process steps include the preparation and creation of the pre-bonding layers, the bonding process itself, the post-bond anneal, and the associated inspection and metrology at each of the steps to ensure a successful bond.

There are two ways in which hybrid bonding can be accomplished: wafer-to-wafer (W2W) and die-to-wafer (D2W) *(Figure 2)*. D2W is the predominant choice for hybrid bonding in heterogeneous integration as it supports different die sizes, different wafer types, and known good die, all of which are generally not possible for W2W schemes. For each, the wafers are first manufactured in a semiconductor fab before a hybrid bonding process is utilized to stack the chips vertically.

Hybrid Bonding Shifts Packaging Toward the "Front-end"

Hybrid bonding takes place in an environment that must satisfy requirements for contamination control, factory automation, and process expertise due to the advanced process requirements and complexity involved – not in a typical packaging house like many other packaging integration methods. To prepare the wafers for bonding, additional front-end semiconductor manufacturing processes are utilized to create the final layers on the wafers to connect the chips. This includes dielectric deposition, patterning, etching, copper deposition, and copper CMP. The semiconductor fab has the requisite environmental cleanliness, process tooling, process control systems, and engineering expertise for the hybrid bonding processes.

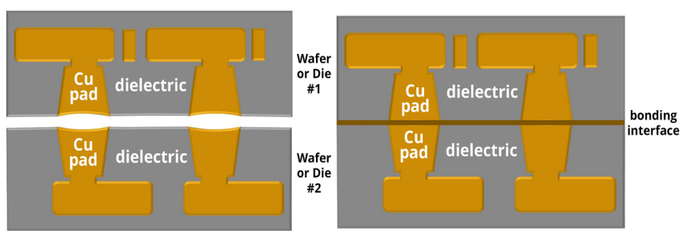


Figure 3: Pre-bonding wafer (or die) image depicting the desired Cu pad dishing profile (left) and a post-bonding image showing a successful die-to-die connection (right)

Known Good Die are Required

Using D2W hybrid bonding to achieve the heterogeneous integration of multiple die into one package results in a high-performance, high-value device. The stakes are high when you consider that including one bad die could cause the entire package to be scrapped down the line. Using only known good die is required for maintaining high yields. Optimization of the process and the implementation of sensitive process control steps are required for achieving die integrity to increase the number of viable die, as well as providing accurate information required to sort good die from bad before entering a process like D2W bonding.

Void-free Bonding for High Yields

Void-free bonding depends upon the successful bonding of both the dielectric areas and copper pads. During the bonding process, the initial bond occurs at the dielectric-to-dielectric interface at room temperature under atmospheric conditions. Subsequently, the copper metal-to-metal connection is formed via annealing and metal diffusion.

The hybrid bonding surfaces must be ultra-clean, as even the tiniest of particles or thinnest of residues could disrupt the process flow and cause device failures. High-sensitivity inspection to find all defects is required to verify that the die surface remains clean for successful void-free bonding.

SiCN has been shown to offer a higher bond strength than alternative dielectrics such as SiN or SiO2. Recent development work[1] has demonstrated plasma-enhanced chemical deposition (PECVD) of SiCN at a temperature low enough to satisfy the limitations of any temporary bonding layer (<200oC). The properties of the film also include the required stability to avoid desorbing hydrogen or hydrocarbons (which can result in void formation) as the temperature is increased for the subsequent copper annealing (>350oC), once the temporary bonding layer has been removed.

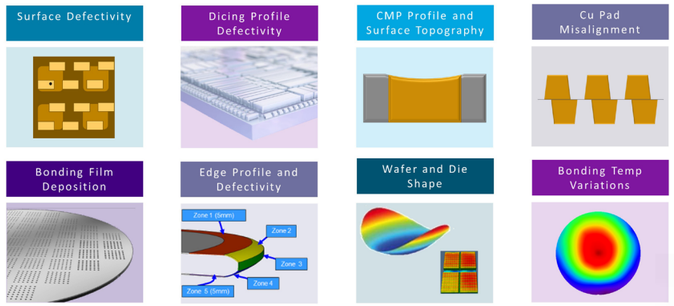


Figure 4: Examples of factors that can adversely impact the hybrid bond quality

Before hybrid bonding, the copper pads must have an optimal, dished profile to allow the copper to expand during the metal bonding process *(Figure 3)*. A shallow and uniform copper recess is necessary to achieve void-free bonding. Here, high-resolution metrology can be used to monitor and drive process control and improvements.

Plasma Dicing for Cleaner, Stronger Die

Many potential sources of voids, defects, and non-uniformities must be carefully controlled at each process step. Even a particle as small as 100nm can result in hundreds of failed connections and a defective stacked package. For example, in the case of D2W hybrid bonding where individual die are diced before being transferred and bonded to a second whole wafer, traditional methods of dicing such as a mechanical saw or laser grooving/dicing can introduce particles or surface imperfections, particularly at the die edges[2], which can interfere with the subsequent hybrid bonding process. Plasma dicing is an alternative method that has already been proven in high-volume production, in specific applications, where the benefits such as more die per wafer or increased die strength outweigh any increased processing costs. In the case of hybrid bonding, the plasma dicing process results in an extremely clean die surface and edge with no particulate contamination or edge chips associated with blade dicing, and no laser debris/recast/laser groove cracks. Plasma dicing die before hybrid bonding will result in more consistent bonding with lower defectivity and higher device yields.

Hybrid Bonding Process Control

To enable hybrid bonding to successfully transition to high volume manufacturing (HVM) with high yield, process control is critical. Pre-bonding non-uniformities across the wafer, voids, and other defects can directly interfere with the copper interconnects during the bonding process and degrade product yield. Additional sources of non-uniformities that impact the bond include CMP profile and surface topography, copper pad misalignment, wafer shape, and variations in bonding temperature. Each of these issues must be carefully measured and controlled at the source *(Figure 4)*.

Some key process control requirements for hybrid bonding include:

- **Film Thickness and Uniformity:** Dielectric film thickness to create the final pre-bonding layers must be carefully controlled, within a die, across the wafer, and wafer to wafer.
- **Overlay Alignment:** To successfully bond surfaces with a very small pitch (currently ~1-10µm), tight control of the bond pad alignment is required to make sure the copper pads to be bonded line up perfectly, driving an increased need for overlay metrology precision and die-bonder control.
- **Defectivity:** The direct dielectric-to-dielectric and copper-to-copper bonds in hybrid bonding require a much cleaner surface free of particles and residues to minimize voiding at the interface. This drives the adoption of optimized processes like plasma dicing along with significantly higher inspection sensitivity and stringent defect reduction efforts compared to conventional solder-bump interfaces.
- **Profile and Roughness:** Successful bonding requires surface profile and roughness controlled to the nanometer level, requiring significantly more precise metrology to help develop and control the preparation of the pre-bonding surface in an HVM environment. Before bonding, the copper pads must have a specific dished profile.
- **Shape and Bow:** Both W2W and D2W hybrid bonding can be sensitive to wafer shape and bow, requiring an increased need for wafer-level and die-level shape metrology for characterization and control.

There are additional process and process control steps required after the actual bonding process, such as inter-die gap fill in D2W bonding where the dielectric is deposited in between, and over the top of the separate bonded die. With appropriate stress control measures, PECVD can produce extremely thick (~30-40µm), crack-free SiO with a TEOS precursor, which is capable of withstanding subsequent steps, such as CMP and lithography.

The scaling to smaller feature sizes and complex 3D integration schemes shifts packaging processes from packaging houses to front-end semiconductor fabs. KLA's wide range of advanced process control and crucial process solutions uniquely help to enable and advance hybrid bonding adoption.

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Excitement Over Chiplets: Not for Everyone and Not Trivial for Test

By Mark Berry, Test Strategies Consultant

Live from "Silicon Desert": The news is all about huge spending by TSMC and Intel. Investment in advanced packaging (2.3/2.5/3D including chiplets) is increasing. As a 5nm design effort tops $500M and photo tools approach $150M, it was necessary to bust up systems-on-chip (SoCs) into re-partitioned systems – where functions that don't need sub 10nm processes are off-boarded to older process nodes, along with specialty technologies beyond core logic (such as PMIC, RF, analog/mixed-signal). A recent high-water mark case making headlines is Intel's Ponte Vecchio (47 active chiplets).

Advanced packaging sources include vertically integrated IDMs, foundries, and OSATs. Chiplet approaches are ideal for some requirements, but they are not for the faint of heart and pose many test challenges. This summary, based on large processor-based systems, will break this down into:

1. Realistic analysis/decision-making,
2. Leveraging standards when forming test plans
3. New work/way (s) forward in test approaches

Realistic Analysis/Decision Making

Many design tradeoffs and test challenges are part of overall decisions around architecture and to what degree chiplets should be used. Test teams must work closely with design and business teams to make decisions to get quality products to market with the right return on investment (ROI). Many test tradeoffs and complexities will help avoid catastrophic surprises such as excessive test times, too many insertions, staffing, lack of coverage, test-related risks that are under-scoped and become issues, and/or schedules that impact time to market.

Chiplet Advantages

- Integration of heterogeneous die
- Higher yield (reduced die size of core- and higher-yielding chiplets based on older nodes)
- Help meet power-performance requirements
- Process large amounts of parallel data with high bandwidth memory (HBM)

Last month R. Zamon summarized a 10nm tipping point.[1] As opposed to intricate chiplet-based systems, a simple system on a board (SoB) with multiple monolithic ICs and SMDs &/or "simple" SiPs can be more effective *(Figure 1)*. Zamon further contends that chiplets produced using older nodes suffer from multiple limitations including performance, latency, heat dissipation, and package size. Chiplets may be new designs, old designs (presumably at older process nodes), 3rd party IP, or derived from other sources (such as a chiplet market). All this makes multi-variate decisions difficult to make.

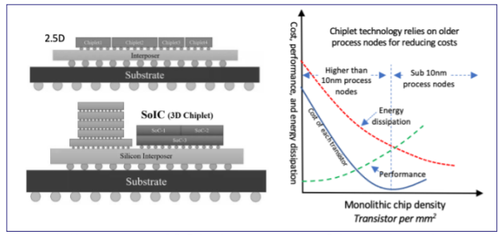

Figure 1: Comparison of 2.5D interposer with a 3D chiplet architecture demonstrates the tipping point of when to move from simple system-in-package (SiP) to more complex chiplets.

Advanced packaging leads to many electrical and reliability issues and risks that will need to be screened out by test and reliability stresses.

Product Risks and Issues Lead to Test Challenges[1,2,3]

- Contact resistance and capacitive loading from pillars and bumps
- Crosstalk and increase noise in substrates and interposers
- Insertion and return losses – especially through-silicon and through-mold vias (TSV, TMV)
- Electro-magnetic effects
- High speed die-to-die interfaces (D2D) are hard to achieve
- Thermal issues with interconnect and underfill layers, bulk silicon, and heat sink
- Mechanical stress of substrates, interposers, die, and package
- Latent defects
- System permutations/options – cores, memory, peripherals in many configurations

Table 1 shows test challenges and a comparison of product types.[3]

Leveraging Standards

Test engineers need to become more fluent with top-down and bottom-up standards. Top-down standards include:

- ODSA – open D2D interface guideline
- UCIe™ - Universal Chip Interconnect Express – see my blog[4] for details
- 3DFabric Alliance – TSMC effort

Bottom-up standards refer to structural and functional methods – some have been around a long time (BIST, scan) but have become more important - others are emerging, such as IEEE 1838.

Test Aspect	Monolithic ICs & Simple SiPs	Advanced Packaging & Chiplets
Access/Pins	Plentiful	Reduced
Ability to Deliver Scan & Configuration Data	Easier	Difficult
DFT Logic	Less stringent and lower impact on area and complexity	Impacts test time, power, area, timing, dev time, scalability
Compatibilities Across ICs in System	Monolithic? – no issue, Simple SiP? - manageable	Challenging
Test Engineers	Typically, experts in RF, mixed-signal, analog, memory, and digital	Hard to come by – multidiscipline experts at the systems level
Observability – Deducing Failure Mechanisms based on Failure Modes	Straightforward	Challenging
Rolled Yield & Coverage	Straightforward	Huge impacts
Inserts	Traditional – probe, final test & QA	Multiple points from KGD probe to sequential steps in assy plus SLT
DFT tools	Adequate	Need advancements - automated test logic implementation, control of interfaces, & pattern gen

Table 1: Test challenges and a comparison of product types.

- IEEE Specifications
  - 1149.x - access ports & boundary scan architecture
  - 1500 - embedded core test(s)
  - 1687 - access to and operation of embedded instrumentation
  - 1838 - die centric standard intended for multi-die packages

Test configurations are then delivered via serial and broadcast networks (1687 & 1500) with 1838 delivery of configuration data through test-access-ports to reach embedded die

New Strategies

Beyond architecture and standards, more invention is needed. There will be a learning curve. Let's look at a few new approaches:

Hierarchical methodology: divide and conquer by dividing the design into smaller hierarchical partitions for quick DFT sign-off (insertion, mode setup, pattern gen, and verification.[3]

- Use package broadcast, on-die scan comparators (ODSC), and "accelerated fly-overs" to leverage re-use, shorten development times, and reduce bring-up overhead.[5]
- Redistribute content such that system-level test (SLT) is performed right after final packaging – then failing units move onto a final test &/or stresses to enable faster learning cycles – good units go on to the final test.[2]
- Accessing and testing die through primary dies with higher pin accessibility using an efficient data delivery mechanism.[3]
- Use a known-good processor and interconnect types from the actual design (silicon bridge, interposer, other) on the load board to test the socketed chiplet DUT.
- On board/in-system telemetry, such as proteanTec
- Greater use of adaptive test, assembly/test monitoring, end-to-end traceability; unit-level traceability for 'big data'; design/fab/packaging/final and system level test real-time adjusts; and comprehensive analytics, such as from PDF Solutions.

Summary

For high-end processors with on-board memory, chiplets offer a way to reduce cost, improve some performance(s) and leverage IP from multiple companies. At the same time – simple wire bond packages continue to make up 70% of the industry's volume and chiplet designs are not always appropriate versus monolithic ICs, simple SiP, and SoB. Realistic analysis and decision-making are needed at the design start – with test considerations in mind. Without this, there can be huge consequences to cost, quality, and time to market. Existing and new standards should be followed closely and as with any new technology introduction, learning cycles and ingenuity are the way. It will be interesting to see how widely chiplet technology is adopted and to what extent it goes beyond the major IDM realm.

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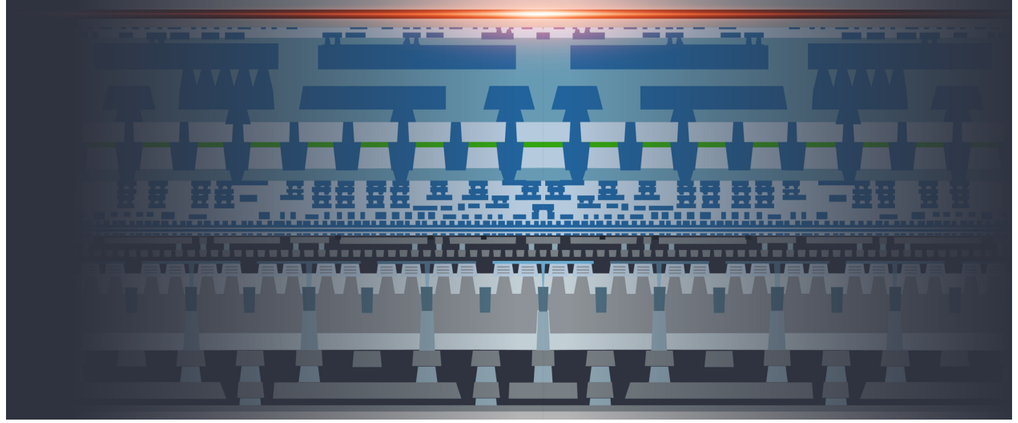

Wafer Bonding and NanoCleave: The New Lithography Scaling

By Thomas Uhrmann, EV Group

In semiconductor manufacturing, 3D integration – the manufacturing, vertical assembly, and packaging of multiple different dies into a single package – is increasingly important in optimizing the power, performance, area, and cost (PPAC) metric in semiconductor design and manufacturing, as well as enabling roadmap continuation. At the same time, wafer bonding is a critical enabler for 3D integration. One can even argue that wafer bonding is the new lithography scaling because without temporary and permanent wafer bonding one cannot vertically stack components and dies *(Figure 1)*.

In the past, 3D integration was driven primarily from a packaging perspective. In other words, different dies on interposers or fan-out wafers were connected to each other, with considerable performance increases. However, the dies were designed and manufactured as a classically 2D system on a chip. Despite enormous efforts and successes in the area of lithography and transistor node reduction, performance increase has slowed down and requires a rethink in the manufacture and design of future processors and memories. Above all, there is no way around 3D integration and wafer bonding or layer transfer.

Moving Beyond Glass Carriers

Carrier technologies utilizing glass substrates, coupled with organic adhesives and wafer bonding processes, have become an established method for building up device layers in 3D devices. The device wafer is temporarily bonded onto the glass carrier wafer using the organic adhesive, where it is then thinned on the backside. Next, an ultraviolet (UV) wavelength laser is used to dissolve the adhesives and release the device layer, which is subsequently permanently bonded onto the final product wafer.

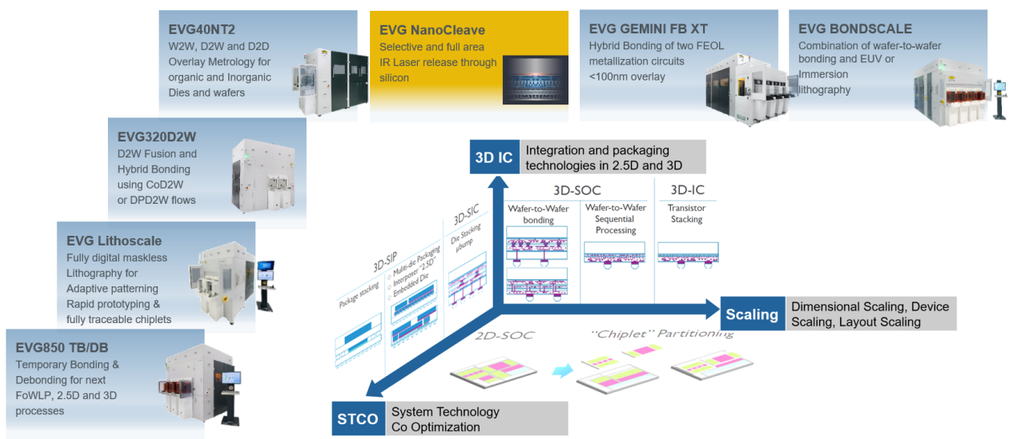

Figure 1: Key industry drivers for improved system performance by scaling, 3D Integration and System Technology Co Optimization.

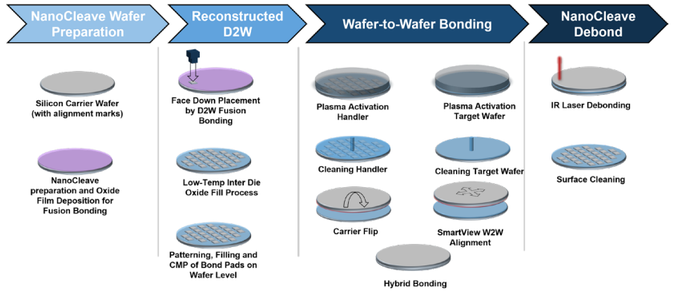

Figure 2: Reconstructed D2W integration combining die placement and processing and reconstruction of ultra-thin chiplets with high bandwidth W2W hybrid bonding.

However, glass substrates are difficult to process with semiconductor fab equipment that has been designed primarily around silicon, and that requires costly upgrades to enable glass wafer processing. Simple things such as wafer edge detection and pre-aligners can be upgraded to make established equipment carrier compatible. More fundamental issues with glass carriers are their electrical and thermal isolation properties, which demand new recipes for deposition or the deposition of extra layers on the wafer backside to allow electrostatic chucking in deposition and etch equipment. In addition, organic adhesives are generally limited to processing temperatures below 300°C, which limits their use in back-end processing.

In a perfect world, fabs could utilize silicon carriers with inorganic release layers to avoid these temperature and glass carrier compatibility issues. Recently, a revolutionary layer transfer approach was introduced that eliminates the need for glass substrates for advanced packaging. This avoids both temperature and glass carrier compatibility issues and enables the ability to transfer ultra-thin (single micron and below) layers via carriers in front-end processing without changing the processes of record.

Revolutionary Infrared Laser Release Technology

This new layer release technology for silicon, called NanoCleave™, utilizes an infrared (IR) laser and specially formulated inorganic release materials to enable laser debonding on silicon with nanometer precision. The backside of the silicon wafer is exposed to the IR laser, which operates at a unique wavelength to which the silicon is transparent. An inorganic release layer that is pre-built into the silicon stack through standard deposition processes absorbs the IR light, resulting in the cleaving of the silicon at a predetermined and precisely defined layer or area.

Utilizing inorganic release layers enables more precise and thinner release layers to be used in the range of a few nanometers versus a few microns for organic adhesives. Subsequent stacking of such thin device layers enables higher bandwidth interconnects, and opens new opportunities to design and segment dies for next-generation high-performance systems. In addition, the inorganic release layers are compatible with high-temperature processing (up to 1000°C), enabling layer transfer for many new front-end applications, such as epitaxy, deposition, and annealing, where organic adhesives are incompatible.

The nanometer-precision of the NanoCleave process supports advanced semiconductor device roadmaps calling for thinner device layers and packages, increased 3D integration, and reduced processing costs through thin-layer transfer and the elimination of glass substrates. At the same time, NanoCleave's compatibility with high-temperature processes enables hybrid and fusion bonding even of ultra-thin layers on silicon carriers, which in turn enables completely novel process flows for 3D IC and 3D sequential integration applications.

For interposers, several improvements in integration and patterning density are on the industry roadmap for leading-edge applications below 500nm line/space patterning resolution. Furthermore, integrated passive devices require high process temperatures (more than 300°C) for dielectric deposition and etching. This is generally unsuitable for adhesive-based carrier systems since the processing temperatures of most thermoplastic and thermoset materials are limited to 270°C.

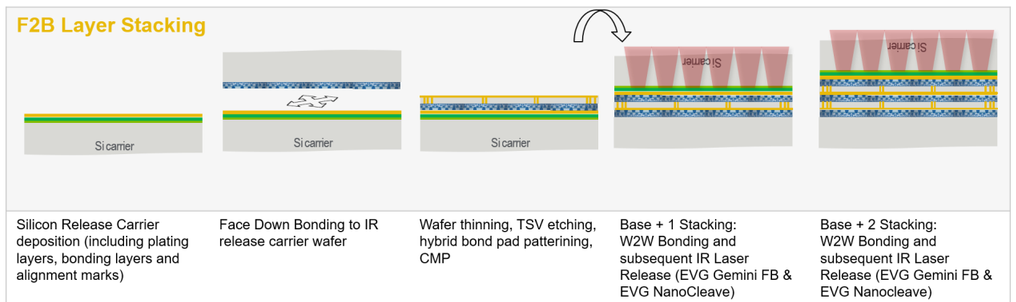

Figure 3: Face to back stacking of ultra-thin wafers on front-end compatible silicon carriers enabled by NanoCleave process.

For fan-out wafer-level-packaging (FOWLP), glass carriers are now standard and meet many requirements of today's packages and interconnect densities down to about 2µm linewidths. However, new concepts are needed to take FOWLP further with linewidths well below 1µm. This is very easy to realize with silicon carriers and IR debond and allows seamless integration of copper and dual damascene.

Enabling Die-to-Wafer Hybrid Bonding

Reconstructed wafers circumvent the restriction of wafer-to-wafer (W2W) bonding by allowing tested good dies to be placed on a carrier substrate and then filling the gap between dies with a dielectric oxide filling process. In this way, a continuous wafer with an oxide surface serves as a base for further process steps. Figure 2 describes the process flow in detail.

One of the main reasons for this process flow is to eliminate traditional packaging materials and replace them with fab-clean and fab-standard materials. This shifts the standard packaging process from back-end-of-line processing to the fab front-end where interconnects are being processed. As a result, more and thinner layers of interconnects in chip processing can be achieved than ever before.

NanoCleave is perfectly suited for enabling silicon as a starting carrier due to the following reasons:

- It provides for a fusion bondable surface to attach chips top side up or bottom side down for mechanical attachment
- It provides the high-temperature capability for all standard fabrication processes at process temperatures of 450°C and higher
- It combines with W2W hybrid bonding to enable layer transfer and uniform stacking of multiple thin wafers, enabling high bandwidth interconnects
- It enables the delamination of ultra-thin films in the sub-micron range

Ultra-thin Layer Transfer and Stacking Using "Temporary" Fusion Bonding

Another significant application of NanoCleave is the combination of IR laser release technology with fusion bonding, which enables fusion bonding to carriers and then area-selective detachment after processing. The IR laser release technology is based on front-end compatible and available materials and deposition processes. This means that there are no limitations in process temperature, that the NanoCleave and release of the product wafer can be conducted without any adaptive process, and that integration flows do not need to be adapted and requalified due to new materials in the line. Another key advantage of using inorganic release layers is their high film uniformity in combination with fusion bonding. As the materials are highly uniform over the wafer and do not alter their properties during processing, the NanoCleave carrier system enables a tremendous reduction in device thickness to sub-micron without damage resulting from the carrier process.

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The Importance of Smart Data Solutions

By Dieter Rathai, DR YIELD

Today, semiconductor manufacturers face more challenges with their data as semiconductors increase in complexity. More sophisticated testing equipment and sensors at every step of the process contribute heavily to the avalanche of data being collected. At the same time, manufacturers are under pressure to increase yields and cut costs.

To achieve the highest yield, reduce the defectivity of semiconductor devices, and solve semiconductor manufacturing problems effectively, semiconductor manufacturers turn to smart data solutions.

In the early years of the Big Data evolution, solutions were created to facilitate data storage, data analysis, and data management. Big Data offers actionable insights from huge amounts of data, with real-time experience, enabling data-driven decisions that save costs and improve products and services.

Yield management solutions (YMS) are designed specifically to meet the needs of semiconductor manufacturers, enabling them to investigate yield excursions, streamline manufacturing processes, optimize the supply chain, analyze tools, and eliminate workplace inefficiencies.

A YMS monitors the entire manufacturing process and provides equipment monitoring and full supply chain visibility. Enhanced data visualization tools give manufacturers deep insight into their manufacturing and test data to uncover patterns and calculate trends and correlations. Automatic anomaly detection can even prevent yield excursions by sending warnings to engineers as soon as an irregularity in the data is detected.

Smart data is data that is condensed into valid, well-defined, and meaningful digital information that expedites information processing. The main task of smart data is to filter out the noise and retain only the valuable data, which can then be effectively used by the company to solve business problems.

In the semiconductor industry, smart data can serve the same purpose as in all other industries. The biggest challenge in terms of data is to quickly identify indicators that can improve yield in the entire manufacturing process. If it were as easy as monitoring a single parameter, there would be no need for smart data solutions.

Not only does smart data filter out irrelevant data and keep only valuable data, but it also sorts and structures the data appropriately so it can be used long past the expiration date of typical data (Figure 1). With smart data, semiconductor manufacturers can reach back into the archives to identify trends, look for anomalies, and make better decisions.

Smart data solutions store, analyze, and manage all semiconductor data collected during manufacturing and test, to improve yields, increase profits and drive innovation, while also playing an integral role in the smart manufacturing environment.

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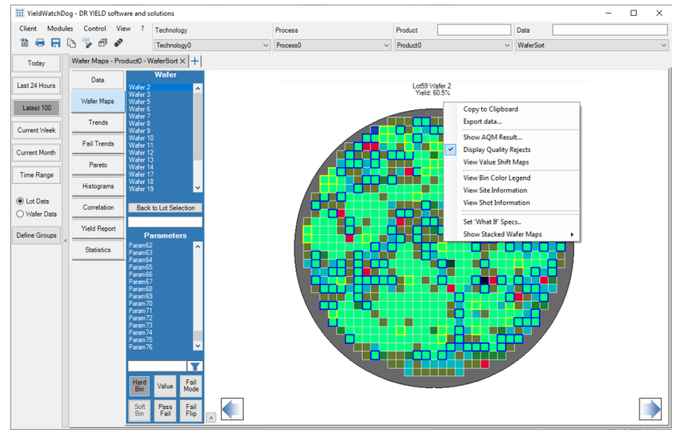

Figure 1: Wafer map sorts and displays quality rejects.

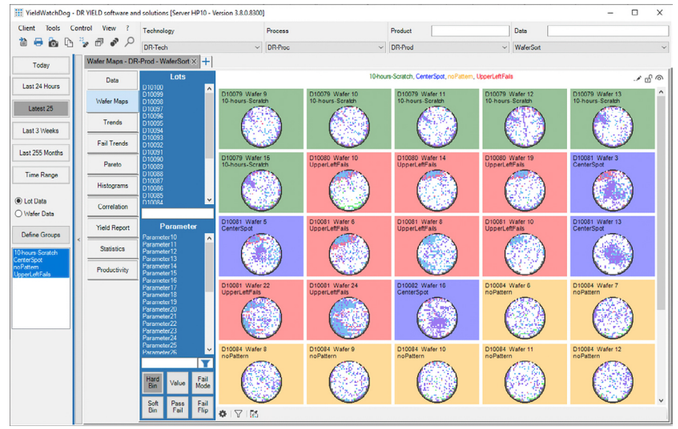

Figure 2: YMS enhanced pattern recognition.

Hiring and Retaining a Diverse Workforce

By Robin Davis, Deca, and Jessica Grafeen, Tektronix

The CHIPS and Science Act aims to bring semiconductor research & development and manufacturing back to U.S. soil. Not only will this make the U.S. less reliant on the international supply chain, but it is estimated that this investment in onshore semiconductor and research facilities will create over half a million new permanent jobs.[1] This growing need to hire generates an amazing opportunity, possibly even a necessity, for companies to look beyond their traditional means of hiring and delve further into diversity and inclusivity to fill vacant positions.

While the CHIPS and Science Act itself includes initiatives to promote diversity, such as a National Science Foundation Chief Diversity Officer and demographic data collection standardization for national agencies, companies will need to think even bigger when it comes to diversity and inclusivity.[2] And they're in luck! Studies show that a diverse workforce improves profitability. For example, "those with more ethnically diverse executive teams are 33 percent more likely to outperform their peers on profitability. Similarly, companies with greater gender diversity among executive teams generated more profitability and value creation than companies with fewer women in executive positions".[3] Companies will need to address recruitment, hiring and retention strategies to not only allow, but encourage, a more diverse candidate pool with more diverse workplace needs.

Re-examine Job Descriptions and Requirements

Assuming that the education side is taken care of, a diverse workforce starts with recruiting. Before even looking for candidates, look at the job requisitions. It's easy to get carried away describing a dream candidate but what is the bare minimum candidate? It may sound counterintuitive to look for a bare minimum candidate, but it widens the recruiting field to include a larger range of skills, knowledge, and backgrounds. It may involve a little more initial investment in training, but a diverse workforce improves problem-solving, which improves the company's bottom line.

"[Earnings] for companies with diverse management teams were nearly 10% higher than for companies with below-average management diversity".4 While reviewing job descriptions, check for any biased language, including coded words and phrases like "compassionate", "decisive," "energetic", and "digital native" that strongly bias towards a particular group. This is also a great time to add a statement about the company's commitment to diversity and inclusivity.[5]

Look for Candidates in New Places

Once there are broader, more welcoming job requisitions, it's time to put them in front of candidates. Traditionally, many companies have offered referral bonuses to get candidates that have already been vetted by current employees. This is a cost-effective way to find "cultural fits" that don't need large training plans; however, this severely limits the ability to increase diversity.6

While it is impractical to do away with referral programs entirely, it is important to look for candidates in places that would otherwise not be reached. Professional organizations and programs targeted at demographics who are underrepresented in the industry, such as the Society of Women Engineers, National Society of Black Engineers, American Indian Science and Engineering Society, and The Mom Project may be a good starting point for recruitment across a more diverse candidate field.

Re-examine Your Hiring and Onboarding Processes

Once the candidate pool is diversified, it's time to take a hard look at the hiring process. According to Glassdoor, "76% of job seekers and employees report that a diverse workforce is an important factor when evaluating companies and job offers."[7] Again, it's important to remove coded and biased language from any actual interview questions. It's also important to remove any rating of a "cultural fit"; when starting to diversify. The goal is specifically to hire outside the current culture of the company. While the idea of work being akin to partying with friends sounds fun, hiring based on "someone you'd like to have a beer with" is unlikely bring a huge diversity.[8]

Beyond the questions themselves, companies can offer additional flexibility within the interview process to demonstrate their commitment to diversity by servicing diverse needs. Allowing candidates some say in the timing, the location (online or onsite), and the formality will allow a broader group of candidates to feel comfortable coming into the interview process.

A little-addressed aspect of retaining a diverse workforce is onboarding. Moving into a more diverse and inclusive workforce means that not everyone has the same background or the same assumptions. This can be a cause of "poor cultural fit" issues, along with other performance-related issues. Good onboarding is an opportunity to clearly state assumptions like core work hours, flexible scheduling, dress code, and even the preferred manner of setting up your outlook calendar or email signature.

Explicitly stating minor cultural choices within an employer can help level the playing field and create an inclusive work environment as it removes unmet, unspoken expectations. This may also be an opportunity to check for bias in these previously unspoken preferences.

Make Them Want to Stay

Finally, the goal is to retain employees for as long as possible. While initial recruiting has a focus on diversifying the candidate pool, retention relies on the equity and inclusivity portion of DE&I. Traditional benefits only go so far; a new set of employees may be better retained with broader benefits.

Looking beyond equality of benefit, ask "What can a company do to provide the equal ability for all employees' ability to achieve success?" Caregiving leave, childcare, and flexible work schedules can make a huge impact. According to a Microsoft UK study, over two-thirds of their staff wanted flexible work hours.[9]

Beyond formal benefits, career development and advancement opportunities are extremely important. Equity comes into play here. Having the equal opportunity to apply to attend a conference does not mean that opportunities are ever given to all employee

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Has Our Industry Become More Sustainable?

By Julia Goldstein, JFLG Communications

The quick answer to the question in this title is "yes and no." There is undoubtedly more talk about sustainability and environmental impact, especially from the larger companies in our industry. SEMICON West devoted an entire day to the topic for the first time. Awards recognizing companies for sustainability are popping up, including **one from 3D InCites** that started in 2021.

But progress sometimes feels incremental, and it isn't necessarily reaching throughout the supply chain. Data show progress toward sustainability goals to back up the talk. Companies in our industry are considering environmental impact when making decisions. Are they doing enough? Let's take a look.

Climate Change and Water Security

One way to gauge the industry is to examine **CDP scores** on climate change and water security. (CDP also has a category for forests, but since semiconductor manufacturing doesn't use a lot of pulp and paper products, that isn't as relevant.)

Table 1 shows 2022 scores for 3D InCites community members, along with other industry leaders that scored an A (the highest ranking) in either climate or water. Ajinomoto and ASE are the only community members to achieve an A. Henkel and TEL are just a little behind. Scores from some members that submitted data were unavailable on the CDP website as of December 2022.

It is nice to see the semiconductor industry represented among the nearly 300 companies that made the A list for climate. It would be better to see more companies up there in 2023 and beyond.

Examining the Community

Companies tend to focus on their small piece of the industry. That makes sense because it is what they know best. We can get a more holistic and complete view by looking at what peers, competitors, and suppliers are doing.

Members of the 3D InCites community represent companies of all sizes and from various sectors, including assembly, design, materials, and equipment. The 58-company list is a snapshot of the semiconductor industry with a focus on packaging. I looked up the member companies to find out what they are saying and doing about sustainability.

Sustainability discussions are becoming more common, but only some are talking. Only one-third of 3D InCites members have a sustainability page on their websites. Even fewer members—22%—issue annual sustainability reports or something similar *(Figure 1)*.

Sustainability reports are often dense documents, with 100 to 200 pages of data and text. Diving into the reports can be confusing. Sometimes data from one section appears to contradict data from another section. I would like to see clearer, more consistent messages. I shouldn't need a conversation with the report authors to determine whether greenhouse emissions decreased or if a reported drop included abatements or offsets.

Progress on Emissions

The companies that issue reports have all reduced greenhouse gas (GHG) emissions per quantity of product or revenue. Some have achieved absolute reductions, which are needed to get to zero emissions. ASE, for example, reported a 3% drop in Scope 1 and Scope 2 emissions from 2020 to 2021 despite nearly 20% revenue growth. That demonstrates significant efficiency improvements, yet the net decrease is still tiny.

Several companies say they intend to achieve net zero emissions by 2040. That goal sounds concrete. The problem is that the path to get there is not clear. The first 20 percent is much easier to cut than the last 20 percent.

Most of the progress is in Scope 1 and Scope 2 emissions. Companies admit that the bulk of emissions are indirect, or Scope 3. Downstream emissions come from using the company's products, which is the most significant contribution for equipment manufacturers. Upstream Scope 3 emissions come from purchased components, materials, and chemicals. Full traceability extends to the extraction and manufacturing of raw materials.

Working with suppliers can help reduce upstream emissions, but control rarely reaches further than one step up the supply chain. As LPKF notes in its sustainability report, "We are as yet unable to comprehensively monitor or control the upstream links in the supply chain."

Waste and Recycling

Henkel states a 2030 goal of "100% of packaging designed for recyclability and reusability" with a caveat. They exempt products where ingredients or residue may affect recyclability or pollute recycling streams. I appreciate the awareness and desire not to pollute recycling streams. What is the plan for those products?

Figure 1: A look at 3D InCites member companies shows how many have sustainability pages on their websites and how many issue annual sustainability reports.

LPKF plans to increase the use of recyclable materials to 80% by 2030. The company is also working to reduce the use of hazardous substances through its annual substitution survey. The goal is to switch to less harmful alternatives wherever possible.

Company	Climate	Water
Ajinomoto Co. Inc.	A	A-
ASE Technology Holding Co.	A-	A
Cadence	B	C
Flex Ltd	A-	A
Henkel	A-	B
KLA	B	C
Lam Research	B	B
Merck KGAA Darmstadt Germany (EMD Electronics in the US)	B	B-
Microsoft	A	A-
Nordic Semiconductor	A	B-
Sk Siltron	A	A-
ST Microelectronics	B	A
TEL	B	A-
TSMC	A-	A

Table 1: How do 3D inCites Community members measure up?

Veeco admits that its waste data is incomplete. It focuses on hazardous waste and does not include office waste or materials sent for single-stream recycling. The company plans to account for its complete waste stream in future reports.

I appreciate the growing awareness of challenges around waste management, including the desire not to pollute recycling streams. I also hope a more comprehensive accounting for waste will highlight the importance of creating less of it. Reuse is always better than sending out hazardous or nonhazardous waste for recycling.

The Upshot

GHG emissions and waste management are only two critical aspects of environmental action. There are signs of progress in other areas. Water reclamation and recycling are on the upswing. Companies are considering how their operations contribute to biodiversity loss and ways to mitigate the impact. The connection between diversity, equity, and inclusion (DEI) and employee engagement around sustainability is building.

My research has revealed progress and also gaps. Awareness about how environmental impact relates to each company's operations has not yet spread throughout the semiconductor industry. Perhaps connections through the 3D InCites community can help broaden the reach.

Creating a Semiconductor Workforce for the Future

By Dean Freeman

There are multiple challenges facing the semiconductor industry as multiple new fabs launch across the United States. A key one is where they are going to get the workforce needed to fully staff and operate them. One challenge is getting students excited again about designing and manufacturing semiconductors. **A recent article** in the South China Morning Post that was referenced in PC Magazine, stated that Chinese students are not interested in pursuing a career in semiconductors. Rather, their focus is on AI and big data because they believe these technologies are clearer prospects.

In India, there have been reports that software classes are being oversubscribed, and students are not signing up for civil or electrical engineering as the jobs are not as prestigious, and salaries aren't as high.

The US has had a similar problem for several years, where the allure of hitting it big at an AI or big data startup has the computer science classes bulging at the seams and electronic engineer tracks in decline *(Figure 1)*.

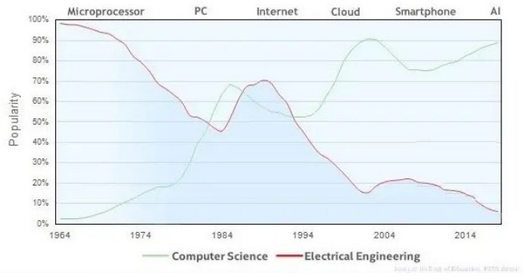

Figure 1: College enrollment comparison of electrical engineering students versus computer science. (Source: The Register)

During IEDM 2022, the evening panel focused on how to draw talent to the semiconductor industry. Theoretical discussions included "how do we bring back the cool" and "how can the industry create a passion for semiconductor technology?" Other suggestions included being more flexible and not limiting candidates to electrical engineers. This was the case through the 1990s, when chemists, physicists, and chemical engineers, were hired along with electrical engineers, and then trained while on the job. People didn't necessarily need a degree to achieve success in the industry. There were many non-degreed engineers and managers on staff at multiple companies, which expanded the potential workforce.

In Korea, both Samsung and Hynix have partnered with universities to ensure a strong workforce by guaranteeing that students will have jobs when they graduate.

Unfortunately, some of the semiconductor industry employment problem is self-inflicted. In the past, the cyclicality of the industry and revenue led to massive layoffs. As a result, some of those engineers sought out employment in more stable fields. This is happening in 2022 and 2023 with the industry slowdown. GlobalFoundries and Intel are either laying off or furloughing staff to cut costs until the next uptick in chip purchasing takes place. There is typically a trickle-down effect so it is likely equipment companies and material companies will also need to furlough staff with this downturn.

Enter the Chips Act

By funding a 200M training initiative for universities and schools, the CHIPS and Science Act provides part of the solution for increasing the microelectronics workforce. This is in addition to $11 billion that also goes to workforce development, other R&D, NSTC, and the NAPMP *(Figure 2)*.

A webinar held by SEMI, BDO, and mySilicon outlined what companies needed to do to obtain CHIPS Act funding. In not so many words, they suggested that working with educational institutions on workforce training would be an important part of the application process. It is probably not a coincidence that most of the new projects are centered around universities with a strong background in microelectronics.

Intel Arizona is partnering with ASU and the University of Arizona. Intel in Ohio is partnering with Ohio State and other universities. Skywater is building a fab in conjunction with Purdue, and Everspin is also building a new facility in Indiana. Micron and GlobalFoundries in New York State are collaborating with SUNY Albany and its nanotech program, along with other strong engineering universities. Samsung near Austin and TI are tapping into North Texas State and other universities close by.

Intel, for instance, has vowed to spend $100 million to improve semiconductor education and research in the United States, and half of that money will go towards trying to line up enough people to work at Intel's manufacturing site in Ohio. in September, **Intel announced** the first phase of funding for its Ohio Semiconductor Education and Research Program and committed $17.7 million over the next three years to fund

National Science Foundation	CHIPS for America Workforce and Education Fund	$200m total	▶ Develop the domestic semiconductor workforce by amplifying activities of the National Science Foundation to promote growth of the semiconductor workforce.
Department of Defense	CHIPS for America Defense Fund	$2bn total	▶ Fund the Microelectronics Commons, a national network for onshore, university-based prototyping, lab-to fab transition of semiconductor technologies.
Department of Commerce	CHIPS for America Direct Incentives + R&D and Workforce Development	$39bn + $11bn = $50bn	▶ Incentivize investment in facilities and equipment in the United States for semiconductor fabrication, assembly, testing, advanced packaging, or R&D. ▶ Implement programs including the NSTC, the NAPMP, and other R&D and workforce development.
Department of State	CHIPS for America International Technology Security & Innovation Fund	$500m total	▶ Support international information and communications technology security and semiconductor supply chain activities.
Department of Commerce	Public Wireless Supply Chain Innovation Fund	$1.5bn total	▶ Spur adoption of open- architecture, software- based wireless technologies.

Figure 2: Breakdown of CHIPS for America Funding for FY 2022-2026. (Source: MySilicon/SEMI/BDO

eight projects, working with more than 80 colleges and universities in Ohio to develop semiconductor education and workforce programs.

Another near-term resource for the semiconductor workforce is the military. Tokyo Electron has launched a partnership with the US Army to help veterans get jobs when they are discharged from the armed forces. Hopefully, the program TEL has initiated will spread across the industry, as a considerable number of these veterans have electro-mechanical experience that could be transferred quickly to a semiconductor facility.

During the IEDM panel discussion, someone asked how the industry can reach down further to high school, and grade school. Multiple robotics competitions take place across the United States each year that span from elementary school to high school. Samsung is in the 13th year of its Samsung Solve for Tomorrow STEM competition, where public school teachers across the U.S. can **apply to the program** by submitting an application that empowers students to inspire real-world change and address some of society's most critical issues using problem-based learning. Lam Research donated to **FIRST® Global**, a nonprofit inspiring science and technology leadership and innovation in young people from all nations through robotics. The contribution, which will be distributed over three years, will help cultivate diverse future talent in science, technology, engineering, and math (STEM). Volunteers from local chapters of the American Vacuum Society (AVS) give demonstrations in elementary schools about how vacuum works. The Intel Foundation supports the **Million Girl's Moonshot** program to equip more than one million girls from under-resourced communities with an engineering mindset.

There is a lot of activity out there simulating STEM activity. What is encouraging is that it has gone from areas that have been associated with a microelectronics community, such as Silicon Valley, to First Global and the Million Girls Moonshot, which provide STEM programs to underserved communities, which will in the long run create a more diverse workforce. Now all the semiconductor community needs to do is work on making the semiconductor industry cool again.

Lam Research's Net Zero Journey Gains Momentum

By Shawn Covell, Lam Research

At Lam, we view environmental, social, and governance programs (ESG) as a business imperative. We focus on improving our communities and the environment and strive to incorporate supportive actions into everything we do – from our operations and workplace practices to how we source our materials and design our products. While our social and governance programs are important and remain a key investment focus for us – let's talk about our planet.

Climate change reports have become increasingly alarming over the past few years. According to the UN Environmental Program's **Emissions Gap Report 2022**, by 2030 the world must cut emissions by 45 percent to avoid catastrophic impacts around the globe. The October 2022 report stated we are far from the Paris Agreement goal of limiting global warming to well below 2°C, preferably 1.5°C, and policies currently in place point to a 2.8°C temperature rise by the end of the century.

While Lam has been making strides in its corporate social responsibility efforts over the past decade, the company's progress on its environmental strategy has ramped up significantly in the last two years. In 2021, Lam announced goals to operate on 100 percent renewable electricity by 2030 and achieve net zero emissions by 2050 – becoming one of the first companies in the semiconductor industry to set such targets.

Determining and Setting Our Goals

The decision to start this journey came from the top: our CEO's direction to the business to establish new sustainability goals, including a target for net zero, was instrumental to where our environmental sustainability program is today. To bring our internal stakeholders up to speed, we held net zero education sessions with the leadership team and engaged with our board of directors. We then used our company's annual strategy and planning process to create the roadmap to achieve our goals. And, to ensure accountability, we created a net zero governance structure with working groups to execute our plans and track progress.

Industry benchmarking was also fundamental from the beginning and continues to play a critical role in our efforts. We reviewed company best practices and aligned our goals with science-based targets to develop our robust strategy. We also leveraged feedback from key stakeholders, which included collaboration with customers.

Igniting an Employee Base

If a company wants to build a genuine climate-aware culture, it needs to have strong governance and active employee engagement. The combination of grassroots passion paired with institutional directives and programs drives meaningful participation across the company.

For the Lam Employee Sustainability Community, their enthusiasm is off the charts. This employee resource group was formalized a year ago and now has chapters in countries around the world with hundreds of members. They have spearheaded significant local projects such as impressive energy and waste reduction programs. Employee resource groups empower employees to take ownership, which is very important because it will take a company-wide effort, engaging employees around the world, to achieve our net zero goal.

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Community Reflections:
The Impact of the EU CHIPS Act, the U.S CHIPS and Science Act, and Beyond

A global trend towards nationalization that began before the COVID-19 pandemic, came to an inflection point because of it. Since then, governments around the globe are realizing the important role semiconductors play in everything from economic leadership to national security. This has sparked a trend in countries and regions investing in the localized semiconductor manufacturing ecosystem.

Two of the most notable government acts in 2022 were the signings of the EU Chips Act, and the US CHIPS and Science Act. As many of our members conduct business from and within these regions, we invited them to contribute reflections on how these events have impacted their companies so far. Here are their answers.

A Small Business Perspective

Paul Balentine, Mosaic Microsystems

As a small U.S. semiconductor packaging company, Mosaic Microsystems is very supportive of the CHIPS Act and looks forward to contributing to the efforts being taken to strengthen the U.S. semiconductor industry.

Our business focuses on the use of glass for substrates and interposers, which are critical technologies required by the industry to maintain a rapid pace of integration and innovation and essential aspects of building a strong U.S. semiconductor supply chain.

Figure 1: Mosaic's CTO, Shelby Nelson, presents the company's technology during the IMAPS DPC 2022 poster session.

With the slowing of Moore's Law, more efforts are being placed on package-level integration. Substrates play a critical role in advanced packaging. AI is pushing the limits of existing high-density interconnect substrates both in terms of feature size and thermal management. 5G is ushering in the era of mm-wave communications, which will require substantial innovations in design, with low-loss substrates playing a key role.

Glass has many properties that make it an attractive material for substrates and interposers. Mosaic's thin glass provides dimensional stability, small vias, and line widths/spacing, smooth surfaces, high resistivity, and low dielectric loss. Having a strong position in glass-based packaging will help the U.S. leapfrog foreign competition.

The CHIPS Act recognizes the critical importance of advanced packaging to the semiconductor industry as well as to the U.S. economy and national defense. While the U.S. accounts for 12% of IC fabrication, it only has 3% of the packaging market and essentially no IC substrate capability. These are Achilles heels for the U.S. There will be substantial investments in packaging from all three major components of the Act – the $39 billion incentives program, the $11 billion R&D program, and the $2 billion DoD ME Commons program.

Mosaic has been active in helping shape these programs by submitting responses to multiple requests for information issued by the Department of Defense and Department of Commerce, attending and participating in industry and government-led symposia, and participating in groups such as the American Semiconductor Innovation Coalition (ASIC). In addition to advocating for investments in packaging in general — and substrates and interposers in particular — we have been advocating for support for small businesses and regional cluster development. Small businesses are an important source of innovation and job growth for the U.S. semiconductor industry.

We have made multiple recommendations to NIST and the DoD on how to support small businesses and startups. As the CHIPS Act funding becomes available, Mosaic plans on having an important role in helping the U.S. build and grow its IC packaging substrate and interposer capabilities. In the Incentives program, we anticipate there will be funding for small businesses that plan to scale.

Mosaic is committed to growing its U.S. glass substrate and interposer manufacturing operations in Rochester, N.Y., and scaling it to high volume. In the R&D program, Mosaic is working with ASIC and other groups to identify technologies and research projects to be funded under the National Advanced Packaging Manufacturing Program. And Mosaic is looking for opportunities to participate in both the Hubs and Cores portions of the ME Commons program. Mosaic looks forward to continuing to help shape and participate in the CHIPS programs.

Ready for US Growth to Address Supply Chain Challenges

Ramakanth Alapati, YES

At YES, we are positioning ourselves for growth that is expected to flow from the on-shoring of semiconductor manufacturing. As a global company, we understand the need for local manufacturing to address supply chain challenges. The governmental incentives persuading large multinational companies to base their manufacturing in the US and Europe are, we believe, simply speeding up a trend that is, in and of itself, a reasonable response to an environment of growing uncertainty.

Figure 2: The YES team exhibited at ECTC 2022 in San Diego.

The return of advanced node logic, memory, and advanced packaging to the United States and Europe, the electrification megatrend-driven growth in compound semiconductors, and the automation of life science products' manufacturing lines continue to underlie the aggressive growth trajectory of YES's business. We see some momentum coming from the CHIPS Act and similar governmental funding programs, but a significant acceleration in disbursing these funds are needed to drive sufficient onshoring of critical semiconductor products to meet the demands of these burgeoning markets.

The past three years have dramatically highlighted the vulnerability of our worldwide supply chains. And although the strictest COVID-related shutdowns are receding into the past, it is safe to say that we have not seen the end of disruptions caused by a changing climate, new pandemics, and a wide range of geopolitical factors still unknown. The increasing pace of economic and technological change will amplify these disruptions. We cannot keep those changes from happening. But as a company, we can be smart about how we prepare for them, and what adaptive decisions we choose to make.

YES has a long and valued history of close relationships with our customers. Indeed, we have defined our company's primary mission as anticipating, enabling, and supporting those customers' technology roadmaps. Establishing physical proximity to those customers is the next logical step in the evolution of that mission, enabling YES to build and nurture stronger connections through changing times.

Consequently, in addition to strengthening our engineering footprint in India and expanding our customer-facing teams in North America, Europe, and Asia, we will be opening the new YES Technology Center in Chandler, Arizona in the first half of 2023. Our Chandler Technology Center is a 123,000-square-foot state-of-the-art facility dedicated to R&D, clean-room operations, advanced manufacturing, and customer support.

As a member of the vibrant "Silicon Desert" semiconductor ecosystem — which includes Intel, TSMC, Infineon, Analog Devices, TEL, and NXP among many others — we look forward to improved communication and greater opportunity for strategic interactions with our key customer base. This geographic hub in Chandler, fueled by the CHIPS Act and excellent support from state and local institutions including the Arizona Commerce Authority and the City of Chandler, is already starting to bring wide-ranging benefits to the semiconductor industry and, by providing a locus for technology innovation, to the world at large.

In summary, while 2023 will likely be challenging from a macroeconomic standpoint, YES is well-positioned to continue our growth trajectory – driven by the on-shoring of semiconductor manufacturing, increasing electrification (particularly in the automotive market), and the ongoing move toward automation of life science manufacturing lines. In support of these efforts, we will continue to invest our resources in increased manufacturing capacity, technology enablement, and customer proximity.

A Once in a Lifetime Opportunity

Paul Lindner, EV Group

Semiconductors truly are the engines that power the world. Yet despite the increasingly prominent role that they play in enabling our everyday lives, until recently semiconductors have flown under the radar for the public. This changed with the arrival of the COVID pandemic, which forced a paradigm shift in how we work, socialize, get our groceries and prescriptions, and even see a doctor.

Maintaining connection with the outside world during COVID lockdowns required consumers to invest in new computers, smartphones, and other various mobile and consumer electronic devices, all of which are powered by

semiconductors. Yet, the dramatic increase in demand for chips during the pandemic caused an unprecedented strain on supply chains that is still being felt to this day. And it's not just PCs with the latest graphics cards that have long delivery times. It's also automobiles, e-bikes, household appliances, and even electric inverters.

Today, governments around the world are beginning to recognize the strategic importance of semiconductors in enabling and supporting our quality of life. This has prompted governments to call for increased investments in domestic semiconductor research and manufacturing to maintain a stable supply chain for consumers, as well as strengthen their national security and global competitiveness. The European Union is acutely aware of this. While one trillion microchips were produced worldwide in 2020, only 10 percent of them were produced in the EU.

Figure 3: The EVG team exhibited at the SEMI 3D System Summit in Dresden, Germany.

The European Chips Act is set to change that. To strengthen the role of the EU in the semiconductor sector, Brussels is investing approximately €43B of public and private money in activities to promote the semiconductor sector. The goal is to double the EU's market share of global semiconductor production to 20 percent by 2030. The next step is for the EU member states and the EU Parliament to discuss and pass the European Chips Act.

Already, we are seeing positive momentum from major chipmakers in expanding manufacturing in Europe. Bosch led the way last year in announcing plans to build a new "smart fab" for microelectronics. Early In 2022, Intel announced plans for an initial investment of more than €33B to build a leading-edge semiconductor fab mega-site and a new R&D design hub, as well as expand existing R&D, manufacturing, foundry services, and back-end production across Europe. More recently, Infineon announced plans to invest €5B to expand 300-mm manufacturing capacity for analog, mixed-signal, and power semiconductors. These and other planned investments in Europe demonstrate that the world's leading technology innovators recognize the importance of Europe as a key center for cutting-edge technology research and manufacturing.

As a leading provider of highly specialized process solutions for the semiconductor industry, EV Group is actively engaged at many levels with the government and industry to share our knowledge and insights on both the challenges and opportunities for Europe's renewal in semiconductor manufacturing. We recognize that an undertaking as significant as the European Chips Act can have a positive impact on our business. However, the European Chips Act means much more to us than that. It is a once-in-a-lifetime opportunity to strengthen innovation throughout the European semiconductor supply chain as well as enhance Europe's technical leadership. We are excited about Europe's "renaissance" in semiconductor manufacturing, and we will continue to work closely with our partners and customers to help guide and support these strategic investments in Europe's future.

A European Perspective Beyond the EU Chips Act

Peter Dijkstra, Trymax Semiconductor

2022 was marked with multiple changes for Trymax Semiconductor Equipment B.V., we moved to a new manufacturing facility, managed supply chain issues, and travel constraints, and implemented a new quality system. Despite all these changes and challenges, we managed to book more orders and ship more systems.

The impact of COVID-19 is still present. In some countries, it disappeared completely while other regions cope with lockdowns on a daily base. From a human point of view, colleagues suffer from long covid and the "normal" five days at the office has changed to 2 -3 days in the office and other days working from home. Public transport is reduced as more people prefer to drive in their own car. This increase in cars created a push for stronger European norms for a clean environment and therefore a strong governmental push for electrical cars.

As a result, we see that the automotive market is growing strongly. Other markets also grow, however at a slower pace. Besides automotive, we also noticed that the storage and availability of data have increased dramatically over the past period and the forecast is very ambitious. People are now used to having high-speed access to data everywhere.

Trymax did benefit from this changing and increasing demand and we've seen a strong increase in IC-Logic (controllers), discrete (power electronics), and optoelectronic (mini and Micro-led) devices. Besides the change in markets, we have also gained more recognition in the market and supplied multiple tools to major OSATs, foundry services, and IDMs. To be able to cope with the increase in demand for systems, it was the right decision to move to a new facility with 27 manufacturing bays instead of seven. The inauguration of the building and the participation of customers and suppliers is still very memorable.

Supply chain concerns have highly impacted the way of working. We increased the interaction with suppliers, and implemented plan B, plan C, and the level of creativity and out-of-the-box actions was, and still is impressive. Hats off to the Trymax team that can satisfy all our customers!

COVID-19 and the enormous pressure on supplying tools are finished, but now another challenge is on the table, the downturn. Different market studies predict a decrease of 15- 22% and yes, the first signs of customers delaying their shipments are already noticeable. I am convinced that 2023 will be another year in which we have to demonstrate our ability to adapt to situations and demonstrate our quality and deliver targets on time.

Finally, I would like to thank, on behalf of the whole Trymax team, customers, and suppliers for the trust and confidence we have received.

Figure 4: The Trymax team exhibited at SEMICON Europa 2022 in Munich, Germany.

Industry Internships Open Doors for The Next-Generation of Semiconductor Engineers

Offering internships is a great way for companies to recruit the next generation of the semiconductor industry workforce. It's a true win-win, as the interns get an inside look at the industry, and companies get to help them fine-tune their skills to meet their requirements. Quite often, those interns sign on as full-time employees.

For the 2022 3D InCites Yearbook, we featured a collection of essays written by the interns who work for 3D InCites Community Members. For 2023, we've continued the tradition. This year's collection includes essays from interns who worked at Brewer Science, ClassOne Technology, KLA, and Trymax Semiconductor.

Cross-disciplinary Experience is Key to Intern Success

By Audra Koch, Brewer Science

As a graduate student in computer science, I was excited to learn about a machine learning internship at Brewer Science. Although much of my coursework has focused on machine learning, I have already learned much more during my internship by applying those algorithms to real-life applications.

During my time at Brewer Science, I experimented with neural networks to analyze the performance of gas and water sensors. One of my greatest challenges was creating a neural network that could work with complex numbers to better reflect the nature of electrical signals.

Although I was intimidated at first since I had practically no background in signal processing or working with imaginary numbers, I became more familiar with these topics through reading books and learning from my coworkers. There's no better feeling than when difficult code finally compiles!

My role has also expanded to that of a "data scientist," which I find is very similar to detective work! Using statistical software, I discovered several interesting patterns in the gas sensor data. After I presented my findings to the team, I realized just how important feedback and collaboration are for finding answers. Understanding the context of the data and how to interpret the results is just as important as knowing the statistical tools, and this knowledge comes only from communication with the domain experts.

Besides learning directly from my coworkers, I felt tremendous freedom in getting to learn from online resources and books. The most surprising thing about my internship is the amount of flexibility I had to learn about whatever interested me, and then I got to use my new knowledge in a way that benefits the company.

Most importantly, I appreciate working for a company that reflects my values. It is evident to me that the number one priority for Brewer Science is the well-being of the employees. The company mission, "A company of the people, by the technology, for the customer, to achieve fulfillment," is backed up by a culture that trusts employees to do good creative work and pays for a 30-minute wellness break every single day. There are also many volunteer opportunities.

This summer, I volunteered at a horse camp called Power of Hope, which provides children with equine therapy. That day connected me to some amazing, compassionate people with a whole new perspective on life. Another thing that surprised me about Brewer Science was its emphasis on art. As someone who works in the tech field, I never thought I would have a company display my paintings at an art exhibit!

Overall, I would highly recommend the internship experience at Brewer Science. The skills I learned here are invaluable, but so are the life lessons I learned from the people. The cross-disciplinary focus and values of the company are some of the reasons I plan to apply for a full-time position after graduation.

Discovering The Semiconductor Industry Through a CAD Tool Internship

By Caleb Dornsbach, ClassOne Technology

Towards the end of my senior year at **Columbia Falls High School**, I was approached by my professor, Dr. Dan Letzow, asking me If I would be interested in an internship working with Solidworks. This internship was at **ClassOne Technology** in Kalispell, Montana. I told him that I was definitely interested in it as I wanted to see other places where CAD is used.

Dr. Dan and I took a tour of one of the buildings and it was really cool to see the tools that make wafers that are used in so many different applications in our day-to-day lives. When I started the internship, I did not really understand the process that went on to create the wafers, however, that would change as I continued to see the parts both virtually and directly by helping in the lab and seeing the machines up close.

Working here has been amazing and everyone was really understanding when I broke my foot. They were very understanding; working around doctor appointments and moving me to the other building so it would not be as far of a drive for me.

Towards the end of the summer, as I was healing, they let me sit in on engineering meetings about developing new tools. It was really cool to see exactly what goes on in the development of new ideas and all the different ideas that are put out there and discussed to see which one or combination of ideas will work the best with the constraints put out for it to work.

Between using a program that I enjoy and seeing the complete process that engineers go through to bring an idea to fruition coming right out of high school was really awesome. I have enjoyed working here at ClassOne as an intern this summer. This is an amazing place to work and has given me extremely valuable real-world experience right out of high school and into the beginning of college.

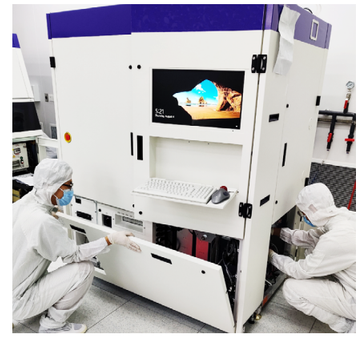
Finding an Engineer's Sense of Achievement at KLA

By Wang Yinghao, KLA

While growing up in China, I was always fascinated by machines and tools and how they benefit our daily lives. My dad worked in the automotive industry, and when our family visited factories, I always enjoyed watching the automated assembly of cars. Starting then, I knew that I wanted to use science to design solutions for societal and industrial challenges like clean energy, increased automation, and autonomous driving.

Knowing that engineers who complete important projects enjoy a great sense of achievement, I decided to study engineering at **Imperial College**, London, U.K. Around November 2020, I started to look for internships.

I was seeking an internship offering real-world engineering experience that would deliver a feeling of achievement by working on actual projects that would impact career growth. Although I interviewed with multiple companies, I focused on **KLA** because the internship presented opportunities to gain direct experience with mechanical design and learn about high-tech manufacturing solutions. I was also impressed by KLA's substantial growth and influential position in the semiconductor industry. My initial interview with the hiring manager was pleasant and collaborative, and I hoped our dialog represented the workplace culture at KLA in Shanghai where I would be based.



From the start of the internship in September 2021, the engineers treated me as a colleague, and I was assigned two projects. For the first one, I worked through a full design process starting with a concept, made 3D models and drawings, ordered parts, and assembled and tested my work. A colleague and I reworked the project, improving small details until we were satisfied with the design.

For the second project, I helped correct, organize and upload engineering drawings for a major

upgrade of a KLA tool, then helped assemble the tool in the cleanroom. As the crated tool was lifted to a truck for shipment to a customer in Singapore, I really felt that feeling of achievement because I had actually seen and touched the tool that emerged from those engineering drawings.

My 11 months at KLA helped to connect knowledge from college with actual work experience in the semiconductor industry. Not only did I gain practical knowledge of cutting, grinding, and drilling in KLA's lab, but I also became skilled at designing parts to meet specific customer needs. And, I improved my communication skills while negotiating with vendors about lead times, part precision, and finishing.

I really valued KLA's workplace interaction. The engineers were very nice and willing to help, often sharing their own experiences. I also joined meetings when team members discussed their own challenges and was impressed by how they shared knowledge to resolve engineering issues. Observing these interactions strengthened my ability to become a successful engineer.

Mindful of each experience during the internship, I returned to Imperial College as a junior in August 2022 with areas to focus on during my studies before I graduate. I hope to earn an MBA and, based on my knowledge and experience at KLA, would like to lead a team of talented engineers to fulfill that childhood ambition of solving problems that make a difference.

Learning About Plasma Technology Hands-on Through an Internship at Trymax

By Mandy Perdok,
Trymax Semiconductor

Hello, I am Mandy Perdok. I am 20 years old and live in Milsbeek in the Netherlands. My hobbies include playing Netball (Team Sport), training/coaching the **Netball** youth team, and traveling.

As a third-year student majoring in Chemical Engineering at the Fontys Hogeschool Eindhoven of Applied Science, I am completing my internship at **Trymax Semiconductors** in Nijmegen.

Trymax was founded by Leo Meijer in 2003. Trymax specializes in designing and building semiconductor equipment for plasma etching. This product line, called NEO, consists of a variety of process chambers and platforms. These range from a semi-automated platform with one process chamber to platforms with multiple process chambers for mass production.

Trymax offers a range of configurable process chambers for plasma technology for all NEO platforms. This allows Trymax to offer a very wide range of processes and options to meet customer requirements.

I enjoy working at Trymax with enthusiastic and helpful colleagues. Furthermore, the support from my supervisors at Trymax and at my university is very good. I was well taken care of by my Trymax supervisor, Kyrill Koekenberg, he also introduced me to the world of Plasma etching. He is an excellent tutor and I learned a lot from him.

As part of my internship at Trymax, I studied the impact of plasma damage on the roughness of wafer surfaces subjected to three materials in three different types of process chambers. The characterization of roughness on the wafer surface is carried out on the basis of a Design of Experiments (DoE).

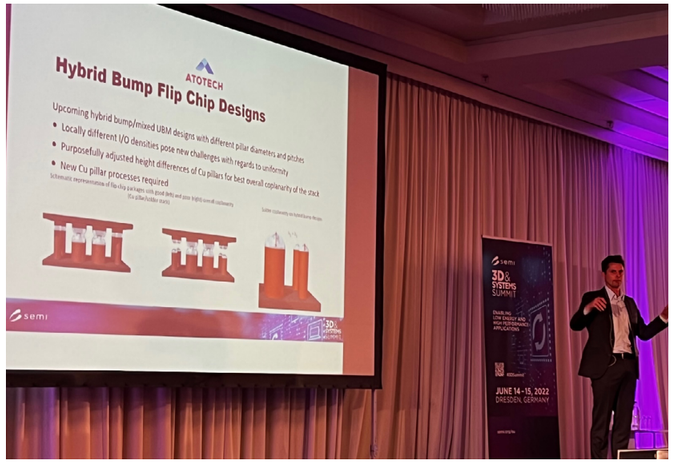
This involves looking at three different plasma reactors and three different wafer layers. The three different plasma reactors include the microwave reactor, the dual source reactor (RF and Microwave), and the CCP reactor. The plasma that is ignited affects the wafer surface. Because three different plasma reactors are used, this means that a different plasma is ignited each time and therefore a different roughness on the wafer surface. The three different wafer layers under investigation are Si, Al, and SiO_2. The process parameters that influence the plasma are temperature, power, pressure, and $\%CF_4$ in the gas mix. Analysis and measurements are done by using STM, AFM, and SEM.

At SEMICON Europa 2022 in Munich, I got acquainted with other companies in the Semiconductor Industry. It was very educational. As a result, my knowledge of the semiconductor industry has been greatly broadened. Also, I had the chance to mix socially with a lot of people.

The semiconductor industry is an interesting and constantly changing Industry. In the future, I would like to do sales in the Semiconductor industry. Furthermore, I hope there will be more women who choose a profession in technology.

2022 IN PICTURES

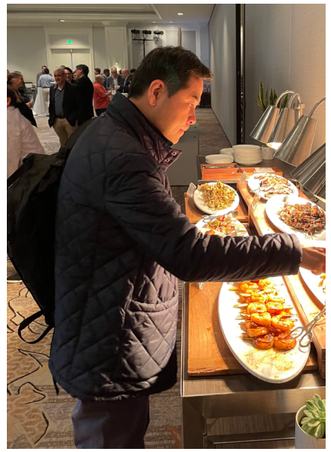
3D & Systems Summit

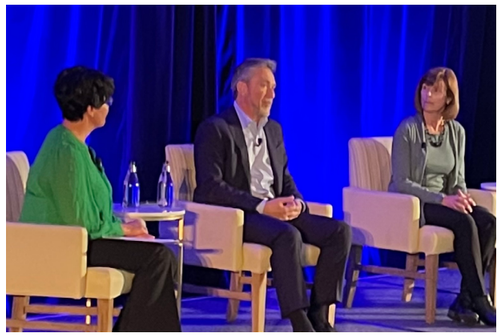


3D InCites Awards

IMAPS Device Packing Conference

ECTC 2022

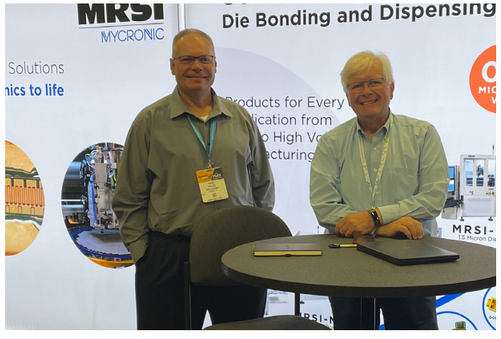


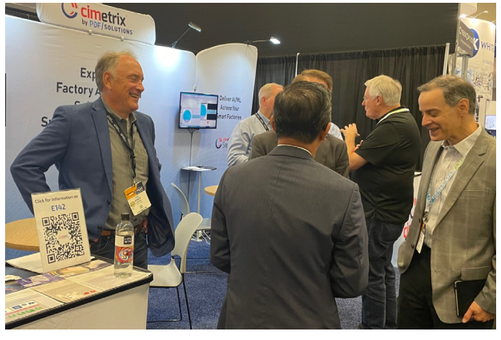


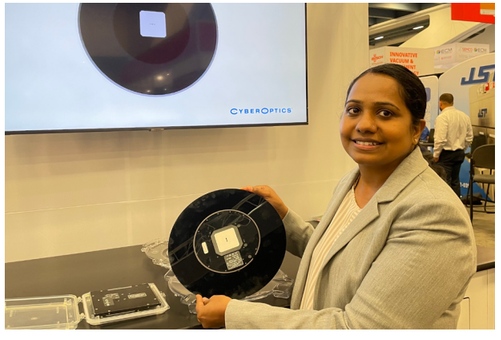
SEMI ISS

IMAPS Advanced SiP Conference

SEMICON West







ESTC 2022

IMAPS Symposium

SEMICON Europa

Wafer Bonding and NanoCleave: The New Lithography Scaling

Continued from page 36

Especially in hybrid bonded memory applications, such as SRAM or DRAM, carrier systems have a crucial role in wafer stacking. To stack the same wafer layouts, without mirroring one of the devices, face-to-back stacking is needed where one device wafer is mounted, thinned and backside processed on a carrier used for hybrid bonding (Figure 3). By freeing any temperature restrictions and enabling ultra-thin silicon processing, through silicon vias of 50µm depth can become through silicon contacts of only a few microns, resulting in improved thermal, electrical, and better cost performance. As a result, NanoCleave carriers are a key enabler for using hybrid bonding on ultra-thin device wafers.

Conclusion

Wafer bonding and layer transfer are critical enablers of 3D integration. Glass carriers and inorganic adhesives have traditionally been used for building up layers in 3D devices. However, continued roadmap scaling requires a new approach to layer transfer technology. A novel and universal IR release technology through silicon wafers, called NanoCleave, has been developed that provides precisely controlled cleaving without IR transmission or risk to the device layer. The use of inorganic IR release layers enables nanometer-precision separation of layers and higher processing temperatures, thereby supporting front-end processing and enabling die and wafer processing with thicknesses below 1µm for improved PPAC. The NanoCleave technology is demo ready at EV Group's Heterogeneous Integration Competence Center™ (HICC) – the company's innovation incubator for heterogeneous device integration – located at its headquarters in Austria.

Beyond today's application, wafer bonding and NanoCleave can play a key role in upcoming device developments by providing a boost to lithography scaling for 3D sequential and even new transistor designs, such as complementary FET (CFET). Further research into this is being investigated.

The Importance of Smart Data Solutions

Continued from page 37

In the highly competitive, high-volume, data-intensive semiconductor industry, with fabs manufacturing at or near capacity, smart data solutions have become indispensable.

Smart data solutions provide a comprehensive solution tailored to the semiconductor manufacturing environment. They compile the enormous amounts of data being collected at every step of the manufacturing and testing process and condense and transform it into valuable, actionable information companies can use.

By combining smart data solutions and AI applications for the semiconductor industry, such as machine learning, predictive analytics, and AI algorithms, a YMS fulfills all the data needs of semiconductor manufacturers. These cutting-edge analytics help manufacturers get the maximum benefit from their data with e.g., automatic pattern recognition, tool combination analytics, and multivariate monitoring (Figure 2).

The key to increasing yield often lies in identifying the combination of factors that contribute to a specific problem or in quickly pinpointing which wafers or lots were affected by a particular issue. A YMS helps uncover these hidden correlations and patterns. Manufacturers using YMS also save on engineering time that normally goes to gathering all the data by making the manufacturing and test data easily accessible.

In short, A YMS created specifically to solve data problems in the semiconductor industry integrates multiple innovative and powerful tools to help manufacturers quickly make smarter decisions.

Hiring and Retaining a Diverse Workforce

Continued from page 39

groups. Employee resource groups and demographic tracking can help promote equity beyond simple equality of opportunity for career development.

In the end, competitive benefits for a truly diverse group may involve creative thinking, data tracking, and even surveys to determine the missing pieces. The CHIPS and Science Act not only brings about funding opportunities for onshore technology development but also an opportunity to bring about meaningful diversity initiatives. To find and retain a more diverse set of employees, companies will need to address not just recruiting and hiring practices, but also onboarding and overall retention benefits. This involves both explicit data collection as well as monitoring for implicit bias in wording, training, and benefits needs. While the initial investment may seem burdensome, studies have shown that a more diverse set of employees brings both creative and financial benefits.

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Lam Research's Net Zero Journey Gains Momentum

Continued from page 44

Continued Steps Toward Sustainability Goals

It was a year of progress for Lam as we unveiled our **net zero roadmap** and marched toward our sustainability goals. Below are highlights of activity in just the last quarter.

- We hosted our inaugural ESG Forum, which brought together our top suppliers to discuss innovative approaches to create a more sustainable supply chain.
- We invited academic and industry leaders to collaborate on solutions that address our industry's most vexing environmental challenges at Lam's **2022 Technical Symposium.** To further our reach and contribute to positive change, Lam Capital sponsored our second startup pitch competition with the theme, "Engineering a Greener Fab."
- The Science Based Targets initiative approved the company's near-term greenhouse gas emissions reduction targets, making Lam the first U.S.-based semiconductor equipment manufacturer to receive this approval.
- Lam joined chip industry leaders to form the Semiconductor Climate Consortium, the first global, ecosystem-wide collaborative of semiconductor companies dedicated to reducing greenhouse gas emissions.
- Lam became a member of the United Nations Global Compact, the world's largest corporate sustainability initiative that calls on companies to act responsibly and collaborate to solve the world's most pressing challenges.
- And for the second year in a row, Lam was named to the Dow Jones Sustainability Index for North America, a ranking by S&P Global that reflects the top 20% of sustainability performers among the 600 largest U.S. and Canadian companies in the S&P Global Broad Market Index.

As we head into 2023, we are focused on meaningful initiatives, continuing to ensure our targets are aligned with current science, and collaborating with organizations around the world to apply best practices. We look forward to sharing our progress along the way as we forge ahead on our ESG journey.

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