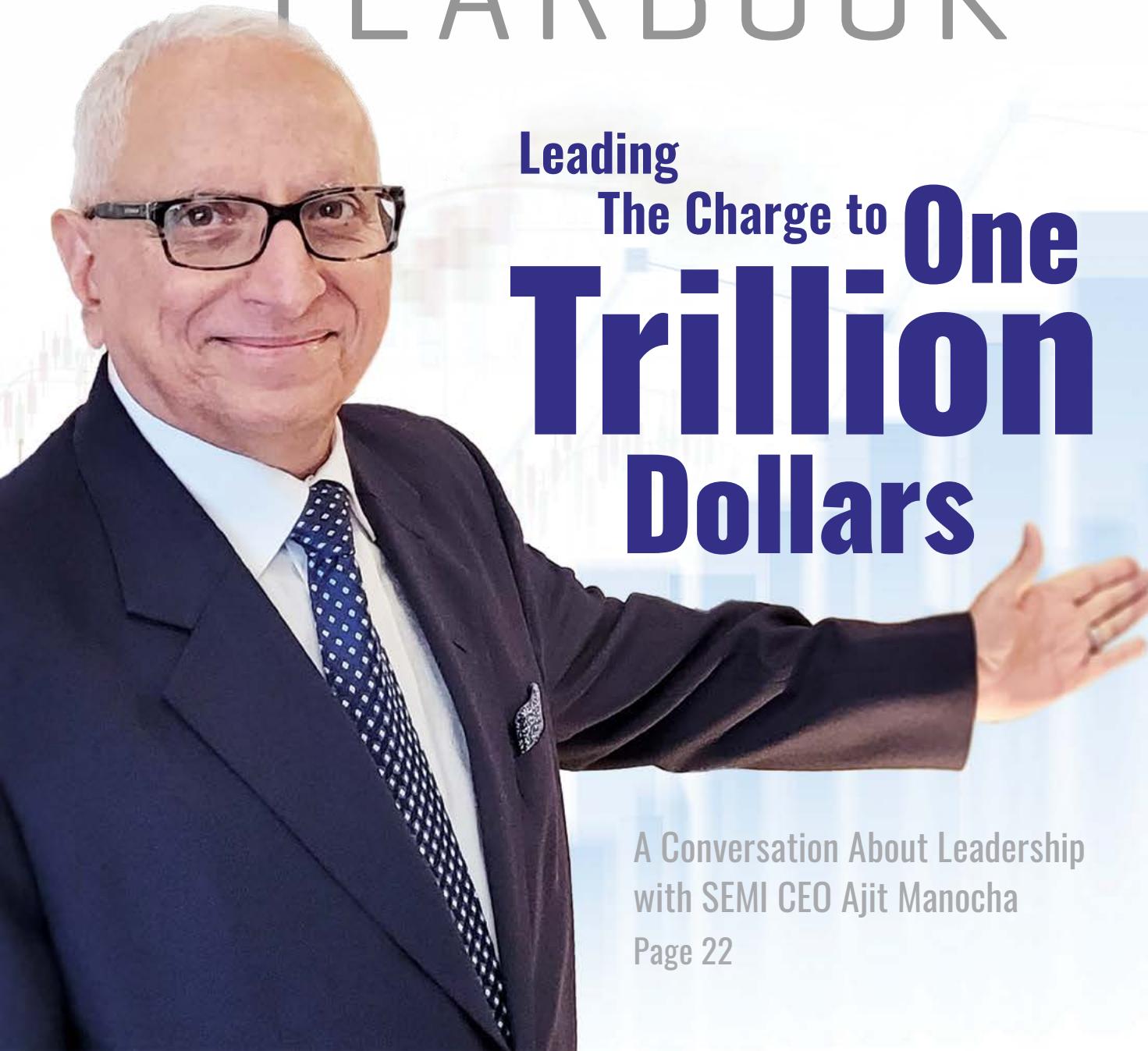




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## YEARBOOK



### Leading The Charge to One Trillion Dollars

A Conversation About Leadership  
with SEMI CEO Ajit Manocha

Page 22

**Page 28**

2024 3D InCites  
Awards Finalists

**Page 50**

Community Reflections:  
How are We Addressing  
the Global Talent Shortage

**Page 54**

The Year in Photos



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# CONTENTS

4 Contributing Authors

7 Editorial: This Is. Community.

22 **ON THE COVER**  
Leading the Charge to One Trillion Dollars:  
A Conversation About Leadership with SEMI CEO Ajit Manocha  
By Françoise von Trapp, 3D InCites

9 Is Our Industry Moving Fast Enough on Sustainability?  
By Julia Goldstein, JLFG Communications

11 The Role of 200mm Manufacturing in Enabling a One Trillion Semiconductor Industry  
By Abdul Lateef, CEO, Plasma-Therm

13 The Semiconductor Cycle: Looking into the Future  
By Dean Freeman, 3D InCites

17 Solving the AI Puzzle  
By Monita Pau, Onto Innovation

20 Driving into the Future: The Next Phase in Automotive Compute Package Adoption  
By Prasad Dhond, Amkor Technology, Inc.

26 Five Workflows for Tackling Heterogeneous Integration of Chiplets for 2.5D/3D  
Kevin Rinebold, Siemens EDA

28 **SPECIAL SECTION**  
2024 3D InCites Awards Finalists

28 Technology Enablement Awards

32 Sustainability Award

33 Adele Hars Award for DEI

35 Best Place To Work Award

36 **EV Group: More than 40 Years of Growth Fueled by 3D/Heterogeneous Integration**  
By Paul Lindner, EV Group

39 The Year in Test  
By Mark Berry, Test Strategies Consultant

40 Thermal Simulation of a Packaged GaN MMIC  
By Casey Krawiec and Erik Sanchez, StratEdge Corporation

42 Balancing Precision and Throughput in 3D Structures with Advanced Packaging and Motion Control  
By David Doyle, HEIDENHAIN

44 When Plasma Matters: Three Reasons to Choose Plasma  
By Peter Dijkstra, Trymax Semiconductor

46 Bridging the Path from University to Industry  
By Rene Dubois, ClassOne Technology

# CONTENTS CONTINUED

48

Semiconductor Industry Marketing and Communications: Learning by Doing

48

Navigating the World of Semiconductors: My Journey at Megatech

By Erwan Amade, Megatech Ltd.

49

Learning About Strategic Semiconductor Communication: My Internship at Kiterocket

By Mindy Lok, Kiterocket

50

## SPECIAL SECTION

3D InCites Community Member Reflections:  
How Are We Addressing the Global Talent Shortage?

50

How Trymax is Navigating the Talent Shortage  
By Tessa Baltussen, Trymax Semiconductor

51

Fostering Innovation from Within  
By Tom Bauer, Onto Innovation

52

Fueling the Workforce Through Investment and Engagement  
By Sophia Oldeide, ERS electronic GmbH

53

Think Globally, Act Locally  
By Paul Ballantine, Mosaic Microsystems

54

2023 In Photos

72

Ad Index

## STAFF

### Françoise von Trapp Editor-in-Chief

Francoise@3DInCites.com  
Ph: 978.340.0773

### Martijn Pierik Publisher

Martijn@3DInCites.com  
Ph: 602.366.5599

### Stephen Wood Director of Operations

stephen@3DInCites.com

### Steffen Kröhnert European Sales

steffen.kroehnert@espat-consulting.com  
Ph: +49 172 7201 472

### Phil Garrou Contributing Editor

PhilGarrou@att.net

### Dean Freeman Contributing Editor

freconsult@gmail.com

### Julia Goldstein Contributing Editor

julia@jlfgoldstein.com

### Trine Pierik Member Events Coordinator

Trine@3DInCites.com  
Ph: 602.366.5696

### Editorial Assistant Sarah Wood

Sarah@3DInCites.com

### Editorial Intern Avery Gerber

averygerber@tamu.edu

### Creative/Production/Online

### Scott Timms Lead Designer

### Ale Moreno Web Developer

### Member Advisory Board

### Dean Freeman FTMA

### Dr. Phil Garrou Microelectronic Consultants of NC, USA

### Julia Freer Goldstein JLFG Communications, LLC

Steffen Kröhnert

ESPAT-Consulting

### Manuela Junghähnel Fraunhofer IZM-ASSID

### Beth Keser

International Microelectronics and  
Packaging Society

### Clemens Schütte

EV Group

### E. Jan Vardaman

TechSearch International, Inc.

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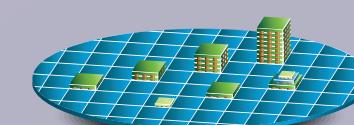
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# CONTRIBUTING AUTHORS



**Tom Bauer**, author of *Fostering Innovation from Within*, serves as vice president of global human resources for Onto Innovation. Tom began his Onto career in 2021, and in his current role, he is responsible for leading Onto's talent strategy

including global talent acquisition, talent management, total rewards strategy, process, and systems. Talent management initiatives led by Tom have resulted in a 40% reduction in attrition over two years through a transparent alignment of organization goals and employee success. Additionally, he built a talent acquisition approach that supported the largest single-year headcount growth in the history of Onto. Tom holds a Bachelor of Science degree in interdisciplinary engineering from Clarkson University and brings over 25 years of experience to the organization.



**Paul Valentine**, the author of *Think Globally, Act Locally*, is the co-founder and President of Mosaic Microsystems. He brings experience in the semiconductor industry from the perspective of private industry, academia, and government. Before

Mosaic, Paul founded CEIS Products, a capital equipment company that reached \$100 million in revenue and was taken public. Paul is also the Executive Director of the Center for Emerging and Innovative Sciences at the University of Rochester. CEIS is funded by New York State to promote economic development through industry-university collaboration and technology transfer. These three experiences give Paul an understanding of ways in which industry, academia, and the government can work together to strengthen the U.S. semiconductor industry through research, manufacturing, supply chain development, government investment, and workforce development.



**Tessa Baltussen**, author of *How Trymax is Navigating the Talent Shortage*, has led the Human Resources Department within Trymax since 2017. She holds a bachelor's degree in Business Management and completed her

MS in Organization Studies.



**Casey Krawiec**, author of *Thermal Simulation of a Packaged GaN MMIC* is Vice President of Global Sales for StratEdge Corporation. He has worked for companies involved with wafer preparation, microelectronic assembly, and packaging for over

25 years. After earning a BS in Mechanical Engineering from the University of Kentucky and an MBA from the University of Louisville, Casey was a design engineer for

the Department of Defense for several years. He began his career in microelectronics at Kyocera, worked for 6½ years at StratEdge, and most recently, was director of sales and marketing at Quik-Pak before returning to StratEdge.



**Mark Berry**, author of *The Year in Test*, is an independent consultant in test strategies, operations, and business development. Past roles included fab-wide photo/etch, device engineering, and product/test ops across all chips in early-generation digital phones (Motorola/Freescale) followed by roles with Amkor and UTAC test with a scope of 5000 testers in 7 countries. Mark has a BSEE from the University of Illinois at Urbana-Champaign & an MBA from St. Edward's University.



**Peter Dijkstra**, the author of *When Plasma Matters: Three Reasons to Choose Plasma*, is Chief Commercial Officer at Trymax Semiconductor. He joined the team in 2021, coming from ASM Pacific Technology, where he served as director of sales, service, and marketing from 2014-2021. Before ASM, Peter spent his career working with plasma-based technologies in the semiconductor equipment space, including ALSI, Nanoplas, Tegal, Alcatel, and the Plasma Physics Research lab.



**Prasad Dhond**, the author of *Driving into the Future: The Next Phase in Automotive Compute Package Adoption*, is Vice President, Wirebond BGA & MLF Products at Amkor Technology, Inc. Prasad joined Amkor in 2014 and is Vice President, Wirebond BGA & MLF Products. He previously managed the Quad and Dual Leadframe product lines. Before joining Amkor, Prasad worked at Texas Instruments for 12 years where he held roles in product definition and marketing in the Analog product group. He holds a BSEE degree from The University of Texas at Austin and an MBA from Southern Methodist University.



**David Doyle**, author of *Balancing Precision and Throughput in 3D Structures with Advanced Packaging and Motion Control*, is the President and Managing Director of Heidenhain Corporation. He joined the firm in 2016, serving as the Vice President of Sales and Marketing. Mr. Doyle has more than 25 years of sales and marketing experience in the international capital equipment business and technical support management.



**Rene Dubois**, the author of *Bridging the Path from University to Industry*, has had a lengthy career in the semiconductor industry, with experience in wet processing, rapid thermal processing and dry etch. His roles have ranged from technical and

field application support to global account management. Rene further honed his account management skills in the industrial market before returning in early 2023 to his career passion for semiconductor equipment at ClassOne Technology.



**Dean W. Freeman**, the author of *The Semiconductor Cycle: Looking Into the Future* is a technology advisor and a twice-monthly contributor to 3D InCites. He covers heterogeneous integration and sustainability topics as they pertain to the greater

semiconductor industry. Dean has over 40 years of life experience in the semiconductor manufacturing and materials space, where he has had experience in nearly every sector of the semiconductor manufacturing process. He has worked both in the fab and for semiconductor equipment manufacturing companies. Dean is also a Subject Matter Expert at Kiterocket. Before joining 3D InCites, Dean was a research VP for Gartner tracking semiconductor manufacturing, process technology, and multiple aspects of the Internet of Things. He has also worked at FSI, Watkins Johnson, Lam Research, and Texas Instruments. Dean has nine process and equipment patents and has written multiple articles in various trade and technical journals. He holds a BS in Chemistry and Earth Science and an MS in Physical Chemistry.



**Julia Goldstein**, author of *Is Our Industry Moving Fast Enough on Sustainability?* is principal at JLFG Communications, LLC. She is a writer and author with a materials science background, trade press experience, and the desire to never

stop learning. Julia writes the monthly Sustainability 101 blogs on 3D InCites. She shares her passion for materials and sustainability in her book *Material Value*, published in 2019. *Material Value* is a B.R.A.G Medallion Honoree, Finalist in the 2019 San Francisco Writers Contest, and Semifinalist for the 2020 Nonfiction BookLife Prize.



**Abdul Lateef**, the author of *The Role of 200mm Manufacturing in Enabling a \$1 Trillion Semiconductor Industry*, is the CEO of Plasma-Therm. He has been with the organization since 1998 and was named the CEO in 2009.

He has since led the organization through strategic growth initiatives, including completing over 10 acquisitions, to grow the company and expand its product portfolio. Abdul serves on the St. Petersburg College Advisory Committee, and he is a leadership coach at the University of Tampa. He founded the Plasma-Therm Foundation, a nonprofit focused on disaster relief and support. Abdul holds bachelor's and master's degrees in Mechanical Engineering from the University of Nebraska and an MBA from the University of Florida.



**Paul Lindner**, author of *EV Group: More than 40 Years of Growth Fueled by 3D/Heterogeneous Integration* is EV Group's executive technology director. He heads the R&D, product and project management, quality management, business development,

and process technology departments. Lindner also leads customer orientation throughout all steps of product development, innovation, and implementation in a production environment. He joined the company in 1988 as a mechanical design engineer and has since pioneered various semiconductor and MEMS processing systems, which have set industry standards. Before he was appointed executive technology director, Lindner established a product management department at EV Group. During that time, he was involved in marketing, sales, manufacturing, and on-site process support.



**Sophia Oldeide**, author of *Fueling the Workforce Through Investment and Engagement* is the Head of Marketing and Communications for ERS electronic GmbH, a manufacturer of thermal management equipment for

Advanced Packaging and wafer probing based in Munich, Germany. She manages editorial and commercial content on behalf of the company, as well as event planning and public relations.



**Monita Pau**, author of *Solving the AI Puzzle*, is a strategic marketing director of advanced packaging, at Onto Innovation. She has 15 years of experience in the semiconductor industry where she has held technical, marketing, and strategic

business development roles in the capital equipment and material sectors of the value chain. Her expertise spans FEOL/BEOL process control solutions, as well as advanced packaging and assembly materials serving both core and specialty semiconductor markets.



**Kevin Rinebold**, author of *Five Workflows for Tackling Heterogeneous Integration of Chiplets for 2.5D/3D*, is a technology manager at Siemens EDA, responsible for its heterogeneous packaging solutions. Kevin is

a high-technology marketing professional with 24 years of experience in product line leadership and business development with a strong electronic design background. Effective communicator with a collaborative, entrepreneurial management style resulting in consistent business plan execution and delivery of industry-leading products. Passionate in working with customers to deliver innovative solutions while identifying new market opportunities to drive product line value and growth.

**Continued on page 70**



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## This. Is. Community.

By Françoise von Trapp



2023 was a year of growth and change for 3D InCites, as well as me personally. In April, I left my role at Kiterocket and the security of a salary and benefits to follow my passion and focus full time on supporting the 3D InCites Community. It was time, and I was ready. We have things to do, and you deserve all my focus. So here I am. Since then, we've grown the membership, rebooted our advisory board to better reflect the community, revamped the 3D InCites Awards, and more.

2023 was all about celebrating the community that 3D InCites has become. As of this writing, we have 62 members and counting. What began as a group of equipment and materials suppliers focused on the adoption of 3D packaging technologies has evolved into a community that represents the entire advanced packaging, heterogeneous integration (HI), 3D HI and Chiplet supply chains.

In 2023 we welcomed Fraunhofer IZM as our first research technology organization (RTO) member, and IBM as the largest North American outsourced semiconductor and test (OSAT) facility. DSV IMS (inventory management solutions) became our first member not involved directly in manufacturing devices, but is a critical element in the supply chain. PulseForge joined after discovering us through their integration partner, ERS electronic GmbH, who is a long-time member. Heidenhain joined because the membership itself represents many of its customers. These are just a few examples.

The pages of this issue are filled with contributed content from our regular bloggers and community members, covering the most critical topics of today. Dean Freeman looks into the future of the **current semiconductor cycle**. Julia Goldstein provides a status check on our industry's **sustainability efforts**, Mark Berry updates us on **test**.

ClassOne shares insights on bridging the path from University to Industry, and several members share their successes in growing their talent pipeline. From the technology perspective, Amkor talks about the next phase of **automotive compute**, Trymax Semiconductor provides tip on when to use **plasma processes**, StratEdge explains the thermal challenges of packaging **GaN devices**, and Siemens shares **five workflows** for tackling HI of chiplets for 2.5D/3D.

HEIDENHAIN explains the **importance of motion control** for today's advanced packaging processes that call for unprecedented speed, accuracy and precision.

While being a community member isn't required to participate in the annual 3D InCites Awards, we're proud to see many members among the finalists, including DECA, ERS, PulseForge, Siemens, LPKF, Multibeam, Zeiss, Cadence, Brewer Science, NAMICS, Onto Innovation, Plasma-Therm, and NHanced Semiconductors. Check out all the finalists beginning on **Page 28**.

This year's cover story features SEMI's Ajit Manocha. In **Leading the Charge to One Trillion Dollars**, Ajit shares his personal leadership learnings to illustrate the approaches we need to take this industry forward and shape a sustainable path to \$1 Trillion.

We've all heard the term "Pillars of the Community". These are prominent members that stand out as key supporters. This year, I'd like to acknowledge three member companies that we consider to be Pillars of the 3D InCites Community: EV Group, KLA, and ASE Group. All three companies have shown their commitment through generous Platinum Sponsorships of the annual 3D InCites Awards for many years.

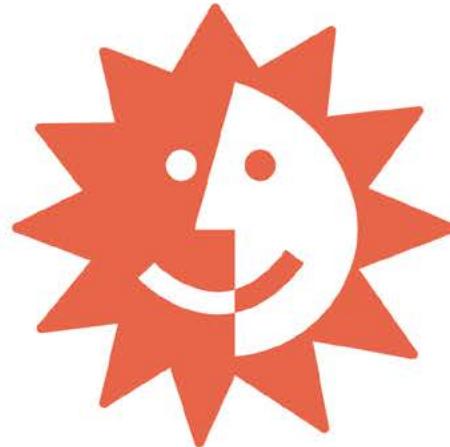
And that's only the beginning. For the third year in a row, KLA will sponsor our now-annual Hike For DEI. This year's proceeds will support STEM education for women and under-represented minorities, through scholarships available at the technical school, community college, and university levels.

For EV Group, the dedication to the community extends beyond sponsorship. EV Group's Director of Marketing Communications, Clemens Schütte joined our newly formed Member Advisory Board and was instrumental in re-shaping the 3D InCites Awards. As EV Group is the OG supporter of 3D InCites before we even had a formal community, I'm thrilled to tap into Clemens' industry and marcom insight.

EVG is a company that fully understands the meaning of community. They've been investing in their local community for more than 40 years. You can read more about the vision of EV Group's founders in the feature article, **EV Group: More than 40 Years of Growth Fueled by 3D/Heterogeneous Integration**, contributed by Paul Lindner.

I could go on... but I'm running out of room. Suffice it to say that I'm honored to lead this community into 2024 and beyond. Remember – you get out of it what you put into it! Let's see where the year takes us! 

*Françoise*



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# Is Our Industry Moving Fast Enough on Sustainability?

By Julia Goldstein, JLFG Communications



We continue to deal with a paradox: semiconductor chips are necessary to support digitalization and society's transition to lower carbon power and transportation. At the same time, semiconductor manufacturing is resource- and energy-intensive. Efficiency improvements are one part of the solution, but they can only take us so far.

What does our industry need to do to reduce absolute greenhouse gas (GHG) emissions to a level compatible with a 1.5 °C rise in global temperature? The answers point to significant challenges. Are we willing and able to completely change some of our processes? That remains to be seen.

## Where We Are

SEMI's Semiconductor Climate Consortium (SCC) is bringing the industry together to discuss environmental issues. As of November 2023, 88 companies have joined as members. The SCC's 2023 report, *Transparency, Ambition, and Collaboration: Advancing the Climate Agenda of the Semiconductor Value Chain*, outlines the current situation and opportunities for improvement.

As the report notes, larger companies have been working on reducing GHG emissions, increasing the use of renewable energy sources, and improving water and waste management for years. Water recovery systems are established throughout the industry and continue to improve.

Still, progress is not fast enough. Even if companies achieve their pledged emissions reductions, the industry is not on target to reach science-based targets for a 1.5°C global temperature rise. Absolute emissions are still going up, in large part due to industry growth. They are not forecast to drop until at least 2030.

I applaud SEMI for gathering companies to collaborate on sustainability initiatives. Awareness is one of the first steps; the report lays out how things look. Everyone in the industry should read it and consider how their company can address its shortcomings in any of the areas the report highlights.

Awareness and discussion are only the first steps, however. We need more aggressive action. We need all companies throughout the supply chain to invest in improvements. That will require changes in design, materials, and processes, increasing R&D expenditure. Those expenses need to be seen as investments in the future of the companies, our industry, and society.

## Looking at Progress

As the SCC report and other analyses have noted, energy use is the change that will make the most difference. That includes switching to renewable electricity to power fabs and other manufacturing facilities and reducing energy consumption. Many companies are already doing this.

Some goals seem overly modest, however. For example, according to its latest sustainability report, ASE pledges to decrease annual power consumption by "more than two percent" by 2030. We can look at that and wonder why they can't do more. There's more to the story, though. In 2022, 87 percent of the company's facilities used some renewable energy.

ASE plans to more than double the percentage of its energy that comes from renewable sources. That's encouraging, but the starting point is 19 percent. Some companies—Intel, Samsung, and others—are already at 100 percent renewables. But many are far behind that. It will take a lot to get the entire industry to 100 percent.

This is merely one example. I could comb through sustainability reports and gather dozens more. The upshot is that companies are doing the work to set goals and report on progress toward them. At the same time, the goals could be more aggressive to encourage revolutionary changes rather than incremental improvements.

## Are Our Hands Tied?

The semiconductor industry faces fundamental limitations in transitioning to renewable power and removing gases with high global warming potential (GWP) from the manufacturing process. Intermittent electricity sources like solar and wind need to be combined with energy storage or other backup sources. Island nations have limited land area for building up solar power. But they also might not be using all the resources available to them.

Process gases remain a major source of Scope 1 emissions. There are some applications where alternatives exist and many where they currently do not. Abatement techniques limit the release of these gases into the atmosphere, but they are not foolproof. A small



portion of gases still escape. The path forward to eliminate the worst-offending gases is not clear. But that doesn't mean we should give up.

Most GHG emissions associated with our industry's products happen during use. We cannot directly influence how end users power their computers, data centers, or automobiles. But we can design semiconductor chips and packages to be as energy-efficient as possible. We can also support improvements in renewable energy in the countries where our facilities operate. That may come from purchasing credits or investing in building renewable power infrastructure.

One point from the SEMI report that people might have overlooked is the call for advocacy. Manufacturers, especially in Asian countries where renewable energy is limited but also elsewhere, should advocate for expanding low-carbon electricity options. If the demand is there, the supply is more likely to follow.

#### Smaller Companies Making Progress

The actions of smaller companies—those with fewer than 1000 employees—don't always make headlines. Our industry needs these companies, many of which make materials and components that contribute to the Scope 3 emissions of the prominent industry leaders, to step up. Fortunately, some are moving sustainability further up the list of priorities.

Namics, for example, is investing in solar farms in Japan and plans to build a solar canopy over the parking lot at

its new headquarters building. Brewer Science purchases enough wind energy credits to cover all the energy consumption at its US facilities. The company's electricity consumption has remained constant despite growth.

Namics and Brewer Science are among the materials suppliers reporting on GHG emissions, energy consumption, and water and waste management. We need more data, along with concerted efforts to promote science-based targets, from every supplier in the industry.

#### The Path Forward

Increasing energy efficiency and transitioning to renewables are the easiest levers to pull and will make the quickest difference. We also need to invest in changes in materials and processes. The journey will take years or perhaps decades. There are ways to accelerate it. That includes supporting promising startups that are innovating in areas like waste recovery, new materials, and energy efficiency.

De-coupling economic growth from energy and resource consumption is something our industry will need to embrace. That's not easy, especially when faced with materiality assessments that show environmental issues lagging behind economic concerns. That can make GHG emissions reductions and better waste management not feel like immediate priorities. Unless customers care deeply enough about their vendors' and suppliers' sustainability records, change is likely not to happen fast enough. A few companies are being proactive and sharing their progress. Here's to hoping that more join in. 



## Accelerate the Future

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# The Role of 200mm Manufacturing in Enabling a \$1 Trillion Semiconductor Industry

By Abdul Lateef, CEO, Plasma-Therm

The global semiconductor industry is growing steadily as integrated circuits (ICs) are now a pervasive part of our everyday lives. Despite recent supply shortages and other challenges, semiconductors are nevertheless projected to become a US\$1 trillion industry by 2030, with more than two-thirds of overall growth expected to be driven by automotive, computing/data storage, and wireless technologies.

While the lion's share of this total will belong to advanced devices manufactured on 300mm and larger wafers, the 200mm manufacturing segment has a vital role to play in helping the industry reach a \$1 trillion valuation. The 200mm and below market is highly segmented, covering many different areas such as power devices, discretes, LEDs, sensors, and others. These areas overlap with the top-level end-market drivers.

For example, in the computing space, what comes to mind initially is leading-edge semiconductors for memory and logic, as they're the primary drivers for computing, followed immediately by chips for artificial intelligence (AI) and big data analytics. From the 200mm perspective, if you are missing the non-leading-edge devices that go around that memory and logic, you still won't have a functioning computer system – thus, while 200mm and below devices in computing may not be enabling, they are essential.

The other top-line end markets are less than 300mm centric. Communication will depend more on RF devices, while in automotive, the fastest-growing semiconductor content is power devices built on compound semiconductors such as silicon carbide (SiC) and gallium nitride (GaN); as well as sensors. For these devices, 200mm and below manufacturing is an enabler; even 300mm content in automotive won't be leading-edge.

The "and below" of "200mm and below" must not be overlooked. Gallium arsenide (GaAs) devices, widely used for LEDs found in optical communications and control systems, are fabricated on 150mm wafers. Moreover, we're not talking about wafers alone – a more accurate descriptor for this market may be "non-300mm," to include panel manufacturing for advanced packaging solutions such as panel-level fan-out devices.

#### 200mm Manufacturing Overcomes Hurdles

There are a few hurdles on the path to \$1 trillion that the industry will need to develop strategies to cope with and/or maneuver around. First is the current geopolitical environment. While this doesn't directly impact non-300mm, as these tools are not on the restricted list, 200mm silicon was neglected for a long time because of the focus on leading-edge devices. Chipmakers' overall strategic planning and investment are now shifting to address the importance of lagging-edge technology nodes, as evidenced by the surge in new 200mm fabs. Transitioning some manufacturing to 200mm and below can ease competitive forces, enabling cost savings and optimized production volumes, helping to drive revenues.

Another hurdle that non-300mm manufacturing can help to mitigate is capacity overinvestment. For years, the global semiconductor industry overinvested first in LED capacity; and then in RF devices. The most recent example is GaAs for RF applications. GaAs fabs are running at a 30-35% utilization rate – primarily because, for every successful GaAs device maker, another three to four fabs have been established, creating overcapacity. The next technology where this could happen again is SiC – the current investment volumes may lead to oversupply in the next few years.

The key takeaway is that investment needs to be more strategic and less reactive. If everyone continues overspending and wasting resources while trying to get to \$1 trillion, it becomes a bigger hurdle. More collaboration in strategic planning would help conquer this challenge – multiple companies coming together to agree on who invests in what over the longer term. This is a tall order, certainly, but it may become a must-do if we are to break the cycle of overspending/oversupply.

Continued on page 69



Figure 1: The chiplet concept disaggregates SoCs to make their functionality more widely available.

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# The Semiconductor Cycle: Looking Into the Future

**Dean W. Freeman**

"It ain't over till it's over." is a frequently used Yogi Berra saying. The current semiconductor cycle has that feeling. While for some parts it appears to be over, for other parts it looks like most segments are at the bottom, and there are no strong growth indicators for the industry.

A bit over a year ago, in the second quarter of 2022, the memory and processor companies were tipping rapidly into a downturn with the first hints of either quarter-over-quarter or year-over-year decline. Companies in the microcontroller and analog space servicing the automotive segment were still seeing flat to positive growth as the automotive space was still experiencing shortages for some chips. The semiconductor equipment industry was still chugging along and would not see the initial impact of the slowdown until either calendar Q1 or Q2 of 2023.

As the semiconductor industry closed out 2023 and moved into 2024 the outlook was still cloudy. Starting in the second quarter of 2023 the memory and leading-edge logic segments started to see positive momentum. Conversely, the microcontroller, analog, and power side of the business looked at a soft Q4 2023. Infineon announced a 5% growth rate for its next fiscal year.



The equipment side of the business gave mixed signals for 2023 of up and down, depending upon which business segment and geographical they are the strongest. The Silicon Industry Association (SIA) data in Figure 1 shows the shape of the last cycle and the start of the rebound as the industry moves into 2024.

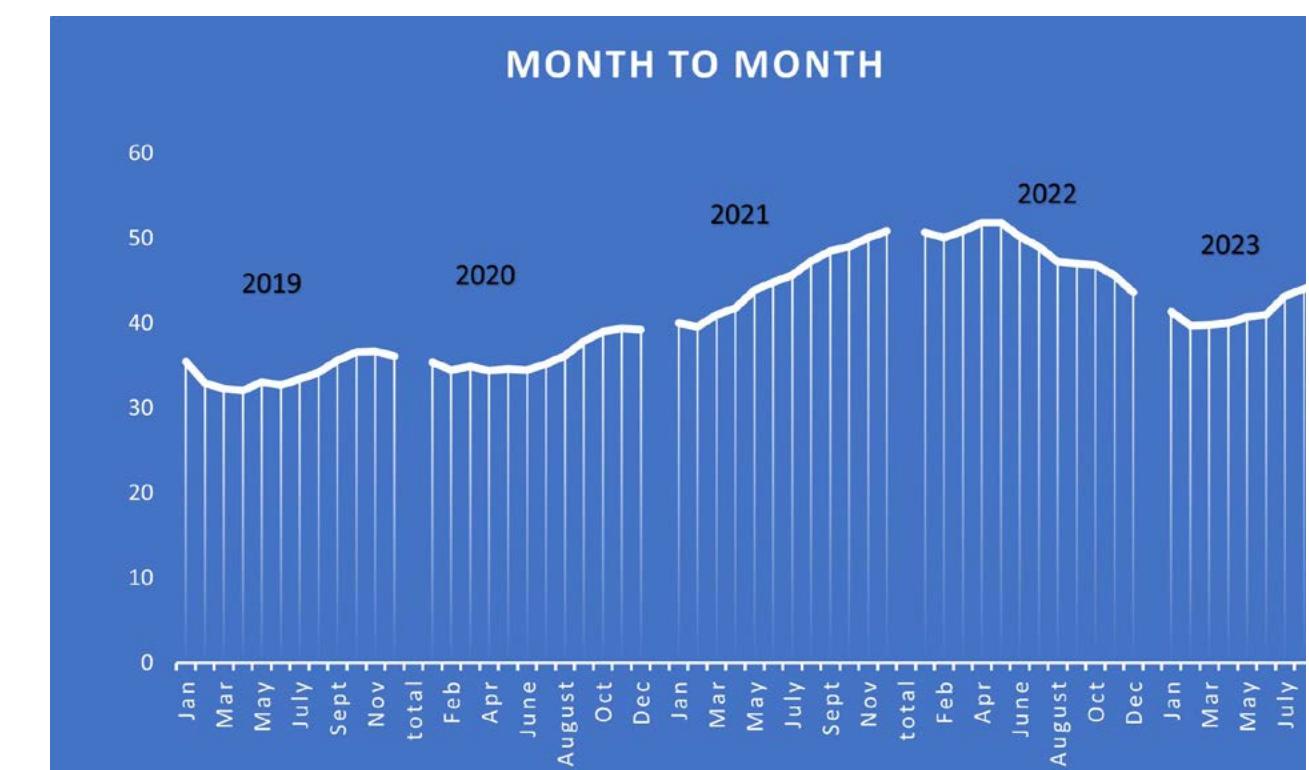


Figure 1. Month-to-Month WSTS data. (Source: WSTS Data)



Depending on your point of view, the current semiconductor cycle started in late 2019, with a brief hiatus due to the pandemic, and then kicked into high gear in the second half of 2021. At its Industry Strategy Symposium (ISS), in 2022, SEMI predicted that \$1 Trillion in revenue for the semiconductor industry was achievable by the end of the decade. As the chart shows in May 2022, month-to-month semiconductor revenues started to decline.

In the November 2022 timeframe, analysts were cautiously optimistic about the downturn. Gartner had a decline of 3.6% and in the **WSTS fall 2022 forecast**, its analysts were predicting a 4.1% decline for 2023. On the equipment side, SEMI was forecasting a decline of 16.8% for 2023.

At ISS 2023, the analyst panel consensus was that semiconductor revenue would decline by approximately 5%. The one exception was Malcolm Penn of Future Horizons, who predicted a 20% decline in semiconductor revenue with a rebound in 2024. On the equipment side, the consensus was a 15% to 22% decline with a rebound in 2024. Mark Thirsk of Linx Consulting predicted a two-year downturn for equipment with a 13% downturn in 2023, and 27% in 2024. For the record, at that time a two-year equipment downturn was looking likely.

### What Actually Happened

Forecasting is an inexact science that depends heavily on your assumptions, as well as your instincts, as no two downturns are alike and something from outside the box can come along and significantly change those assumptions. What happened in 2023 and where does it look like the industry is headed for 2024?

Two of the many assumptions for 2023 were that China would see a strong second-half recovery and that 5G and China would help to drive mobile phone purchases and thus provide some bright spots during the year. These assumptions would help memory recover, and drive some logic revenue. Neither of these assumptions came to be. As a result, memory prices continued to decline throughout most of the year, only stabilizing when inventories had been worked through or written off, resulting in a revenue decline of greater than 30% for the segment dependent upon Q4 23 growth. Companies building computer and mobile processors also saw greater than a 10% decline in revenues for those segments with 10% being the high side.

### Bright Spots in High Bandwidth Memory

The key positive drivers for memory in 2023 were high-bandwidth memory (HBM) for artificial intelligence (AI), and automotive applications. AI and automotive were segments that had positive growth across the industry. For microcontroller units (MCU) and power chip manufacturers, automotive and electrification led to a positive year for most of those manufacturers.

This led to a bit of an unusual year where the MCU and analog manufacturers reported growth, while the memory and PC and mobile logic manufacturers headed

for a negative year from a growth perspective. Typically, when there is a downturn, revenues are down across the board, so the automotive and power semiconductor growth is one of the unique aspects of this cycle. As renewables drive the electrification of the grid and the electric vehicle (EV) market continues to grow, it will be interesting to see if the automotive and power semiconductor industries continue to have a different cycle than the computing and consumer segments.

In the equipment segment, there were significant pushouts at the leading edge in 2023. There were also delays with the first TSMC fab in Phoenix. The restrictions in China also had an impact, but not as significant as first feared, and some equipment companies had great years in China. In China and the world, the power, automotive, communication, industrial, and IoT segments kept on purchasing equipment.

According to **Trend Force**, in China, there are currently 22 or 23 fabs in different phases of construction and 10 more planned. The bulk of these are projected to be 28nm and above with fifteen 300mm and eight 200mm (Figure 2). This is a significant amount of equipment as some of these fabs, when completed, will be running 100,000 wafer starts per month. Depending upon the equipment sanctions, China's manufacturing growth will continue to be a driver for equipment sales during this next cycle. Silicon Carbide (SiC) for electrification and EV will be a key growth area for 200mm fabs.

### Will We See Growth in 2024?

Where does it look like the industry will end up in 2023 and what are the assumptions for growth in 2024? When writing this article, the latest published SIA numbers ran through September of 2023. The chip industry needs to see approximately 4% growth quarter-over-quarter to hit the **WSTS forecast** of a 10% decline. This would put chip revenues at \$515 billion for 2023. Q3 revenue grew 10% over Q2 so hopefully it's safe to say that there is an opportunity for some upside to those numbers and the year will end a little better than currently forecasted.

On the equipment front for the top few companies, **revenue growth looks** like it will range from positive 29% growth to a 25% decline, so now it will be challenging to determine where equipment will end up for 2023 until the final numbers are in. The Chinese equipment companies are having a banner year, which will also help the year-end number. For the fourth quarter of the 2023 calendar year, ASML is forecasting a positive 4% growth in Q4 over Q3. Other equipment companies are forecasting flat to slightly down growth for Q4 calendar year 2023. So, while chip revenues are improving, it looks like the equipment segment is taking a short breather as it moves into 2024.

For 2024 the most recent forecast on the chip market is by IDC predicting a 20.2% growth. The WSTS spring forecast predicted 11% growth for 2024, which will likely see an upgrade in the fall 2023 report. Other reports are starting to emerge, and currently, they are falling in between the above predictions.

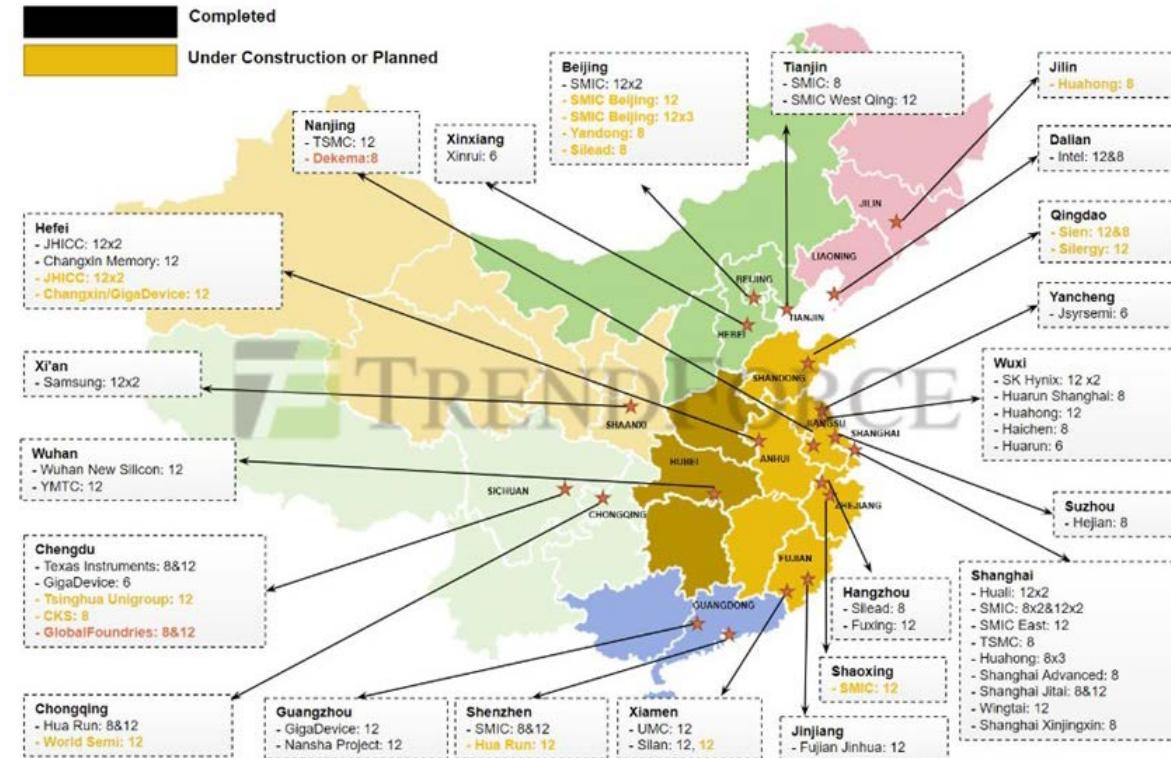


Figure 2: Map of new fabs being constructed in China. (Source: Trend Force China Fab Analysis.)

### Key Drivers for Recovery

What are the key drivers for the recovery? According to the most recent Gartner forecast, IT spending will increase by eight percent. Data center systems are the biggest driver with 9.5% growth year-over-year as cloud and AI data centers continue to expand. The PC market is expected to be at 4.9% growth according to Gartner. Mobile phone growth will be in the same vicinity depending upon the success of the recently released models.

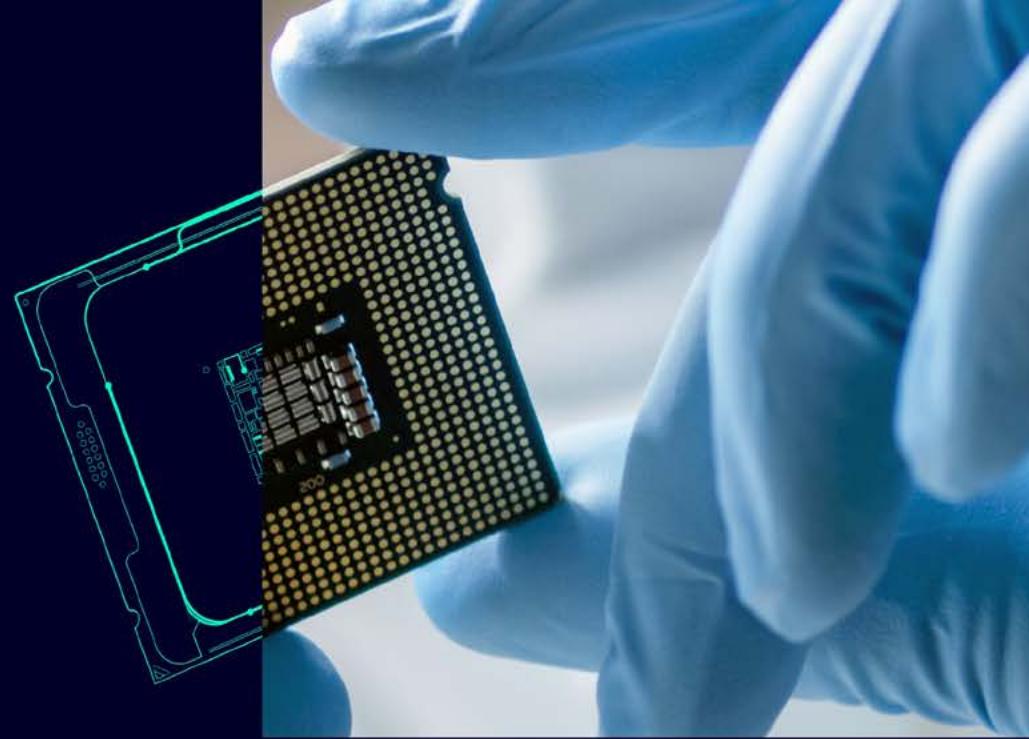
Increases at the system level will drive chip growth but, how does the chip industry get to 20% growth? From a chip perspective, the stronger asking selling price (ASP) for HBM DRAM, and higher performance DRAM for systems such as EV, will be the key driver for memory growth. NAND is expected to see growth later in the year as the need for storage grows.

Prior to and in the Q3 earnings announcements, Intel, AMD, QUALCOMM, Samsung, and Nvidia discussed processors for a new AI-enabled PC and AI mobile applications that would become available in 2024. These new devices would use a processor designed to enable personal AI performance and move AI from the cloud to the local device. Depending upon the demand, these new devices could be a market driver for higher-end chips with higher ASPs before the end of 2024. The question to ask is whether industries or consumers are enticed to purchase these new PCs and mobile devices.

On the equipment side, demand will be driven by equipping the new advanced fabs coming online in 2024 and 2025. China will likely continue to have strong demand for equipping its fabs. A key part of the equation is how fast will the capacity that has been taken offline during this downturn get re-adsorbed. Foundry utilization rates are currently in the 70% range and it is likely that the memory fab utilization is in a similar range. Thus, the equipment forecast for 2024 depends heavily on end demand and improving fab utilization before equipment purchases will see a significant pickup.

While chip forecasts in the fourth quarter will likely come out in the 10-20% range, due to what seems a stronger-than-expected 2023 for semiconductor manufacturing equipment, it's possible that equipment sales will start the year slow, and then begin to ramp in the second half of 2024, ending the year close to the positive 10% number that has been predicted. However, there are a lot of assumptions that must fall into place for that to happen. In the third quarter of 2023, consumer spending was slowing. Analysts will need to determine if this trend continues into 2024 as they make up their forecasts.

Yogi Berra also is reported to have said it's tough to make predictions, especially about the future. I expect 2024 to be one of those years until the drivers for growth clearly emerge.



# Facing semiconductor scaling challenges?

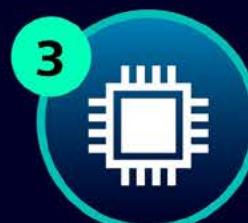
These **5 key workflows for 3D IC** deliver the heterogeneous integration (HI) of chiplets necessary for 2.5D/3D design. Explore and deliver product differentiation faster using Siemens EDA's market-leading 3D IC technology solutions for 3D heterogeneous integration of node and performance-optimized chiplets.



1  
Architectural Planning & Analysis



2  
Physical Design Planning & Analysis



3  
Design Analysis

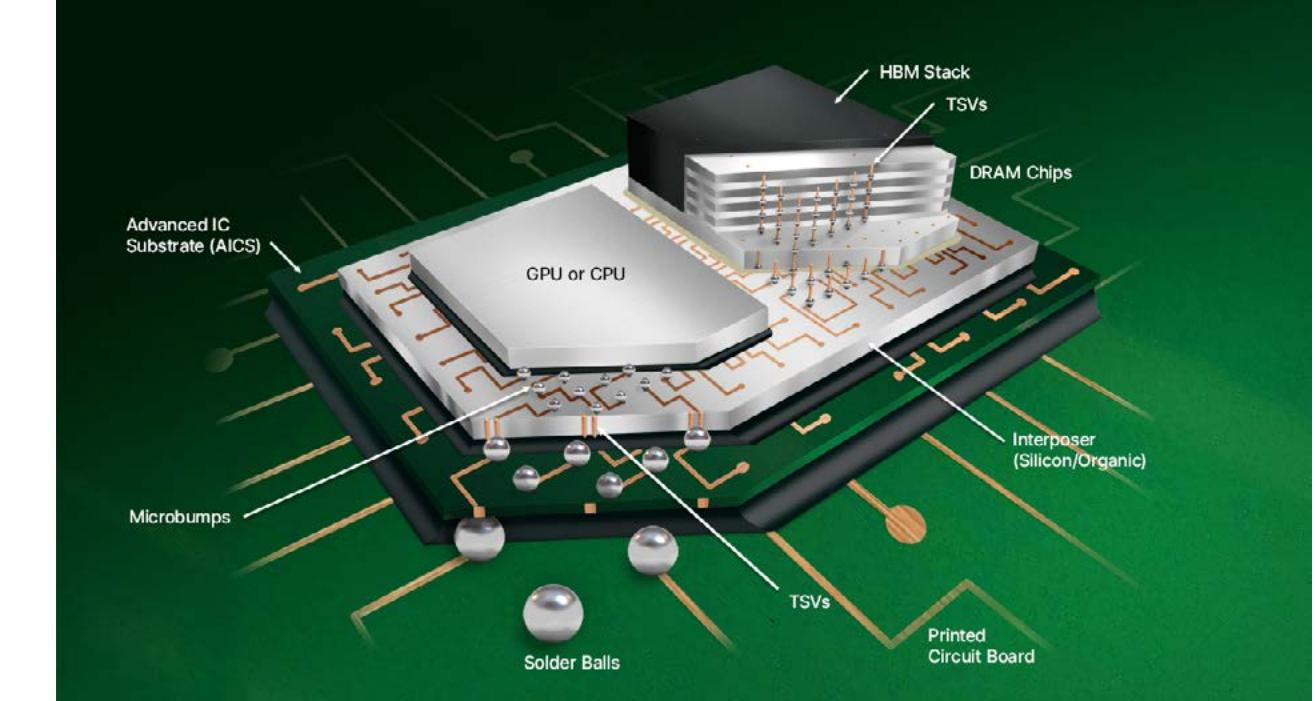


4  
Reliability Analysis



5  
Test Planning & Validation

Your complete solution for  
2.5/3D IC  
packaging  
design and  
verification



## Solving the AI Puzzle

By Monita Pau, Onto Innovation

An AI package is like a puzzle made up of individual pieces of different sizes and shapes, each one essential to the final product. Together, these pieces are typically integrated in a 2.5D IC package designed to reduce footprint and maximize bandwidth.

A graphic processing unit (GPU) and multiple 3D high-bandwidth memory (HBM) stacks provide the major pieces in the AI puzzle. These puzzle pieces are first assembled on top of a silicon interposer. An advanced IC substrate (AICS) provides the foundation on which the 2.5D package is built.

While we could go on at great lengths to discuss the manufacturing of each of these AI puzzle pieces, for this article, we are focusing on the advanced packaging side of the process – the glue that holds all the pieces together – and the many manufacturing challenges of a 2.5D IC package.

But before we get into that, let's talk about what AI is and what AI isn't.

### A Word About AI

Forget what the movies have told us. AI today has little in common with sentient machines dedicated to serving or enslaving humanity. As we know it, AI is simply a new type of technological tool. It does what other tools do: enables its users to complete tasks with more efficiency and ease. The following is a list of the different types of AI, a list that, fittingly, was created using generative AI.

**Artificial Intelligence (AI):** This is a broad term that encompasses all aspects of creating intelligent

machines. AI is used to classify machines that mimic human intelligence and human cognitive functions like problem-solving and learning.

**Generative AI:** This subset of artificial intelligence uses techniques (such as deep learning) to generate new content. For example, you can use generative AI to create images, text, or audio.

**Machine Learning (ML):** This subset of AI focuses on prediction and classification tasks. Machine learning is AI that can automatically adapt with minimal human interference.

**Deep Learning:** This is a subfield of machine learning that uses artificial neural networks to mimic the learning process of the human brain. It focuses on neural networks to solve complex problems.

Each one of the above applications benefits from or needs high-performance computing capability.

Now that we have discussed AI let's explore the packaging challenges of 2.5D AI devices further. This article will focus on the challenges associated with through-silicon vias (TSVs), microbumps, and AICS.

### TSV Challenges

TSVs are a key piece of the puzzle for the construction and performance of both 2.5D and 3D packages. Designed with extremely small critical dimensions, high-aspect ratios (HAR), and fine pitches, TSVs enable high numbers of inputs/outputs and provide vertical electrical pathways for HBM and silicon interposers (Figure 1).

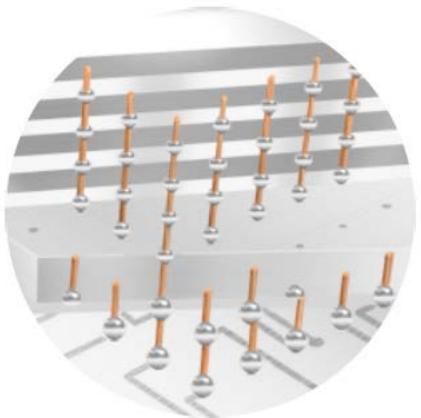


Figure 1: Depiction of high aspect ratio through silicon vias.

The TSV process is intensive and requires several key process steps, including etch, deposition, fill, and chemical mechanical planarization (CMP). With the demand for thinner silicon die, decreasing TSV size, and, in some cases, even higher aspect ratios, controlling the exact size and depth and finding increasingly hidden defects, is essential to maintaining high yield.

Top and bottom critical dimension (CD), sidewall profile, and depth are all important process control parameters for TSV manufacturing, as they can affect electrical performance between the stacked die. If the TSV is not etched deep enough, the two dies will not be connected even if they have been placed on top of each other. Next, the barrier/liner material is deposited with good uniformity and thickness control. Electro-plated Cu fills the TSV, where measuring the overburden thickness — as well as inspecting the Cu fill for growth defects and voids — is critical.

As for the backside of the wafer, the front of the wafer will be temporarily bonded to a carrier so the backside can be thinned to reveal the TSVs. The thinning process is important. The remaining silicon of the etched TSV must be measured and monitored for grind and blanket etch to ensure TSV interconnects are evenly revealed for stacking the chip or entire wafer. Failure to accurately measure and inspect the backside can lead to defects, distortions, electrical resistance, and device failure, which ultimately leads to increased scrap and decreased yield.

Tools that are useful to address the above challenges include metrology for advanced OCD and HAR structures and an automated high-speed sub-micron defect inspection and 2D/3D metrology system.

#### Microbump Challenges

In addition to TSVs, microbumps are also a key element providing the interconnections between the different components within the AI package. Besides connecting the individual DRAM layers and the logic buffer die within the HBM stack, microbumps connect the 3D memory stacks and the GPU to the interposer. Larger solder bumps also connect the interposer to the advanced IC substrate (AICS) (Figure 2).

Much like TSVs, microbump technology continues to scale downward, decreasing height, diameter, and pitch. Further shrinking is expected and eventually calls for using direct Cu-Cu hybrid bonding. A primary downside of this shrinkage is maintaining plating uniformity of the bump — both within the die and across the whole wafer. This becomes more challenging. For the die to properly attach to the next component — whether it is DRAM, logic buffer die, interposer, or IC substrate — these bumps need to be the same height to ensure proper connections.

Measuring the individual thicknesses of each of the metal films used to construct the bump is also important. The choice of metal and its respective thickness are critical in controlling the performance and reliability of the device.

Another potential stumbling block with microbumps is related to defectivity: the presence of residues, cracks, voids or to an even greater extent, where the microbump is damaged or displaced. In extreme cases, these defects result in immediate electrical shorts or failed connections. However, the impact of some of these defects may not be apparent at first but slowly evolve over time and affect device reliability.

Each of these challenges, if not properly addressed, will impact device performance. An opto-acoustic metrology tool using picosecond ultrasonic technology can measure both individual metal film thickness and the final total bump height. A combination of 2D/3D metrology and inspection tools can measure bump diameter and bump height, as well as detect defects, delivering in-line process control.

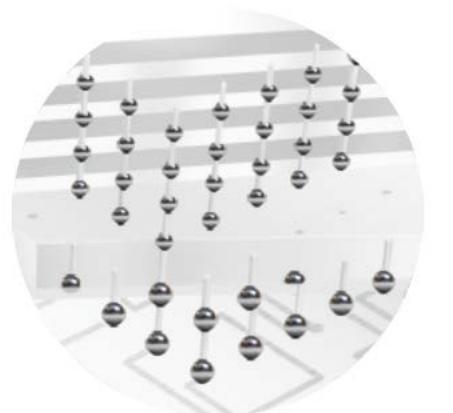


Figure 2: Focus on microbumps.

#### AICS Challenges

As input/output (I/O) density increases, the ability of individual components to mate directly to the printed circuit board becomes an issue. This is where AICS enters the process as a piece of the AI puzzle. AICS acts as the bridge between the package's individual components (Figure 3). To connect the interposer above — and the die connected to it — a high number of redistribution layers (RDL) are needed. As the number of RDL layers increases, so does the possibility of overlay errors.

Speaking of RDLs, a large landing pad at the end of each interconnecting line/space (L/S) connects to the vias. The landing pad is significantly larger than the critical dimension of the RDL. This helps increase overlay tolerance. However, these large landing pads limit design space. This problem will only be exacerbated as the interconnect technology demands finer L/S. This results in the need to increase the number of RDL layers, along with an increase in cost and potential yield loss.

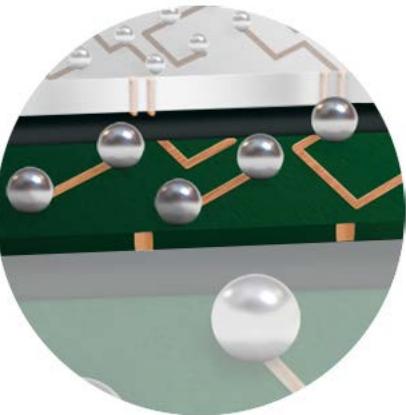


Figure 3: Focus on advanced IC substrates.

To mitigate this design quandary, smaller RDL landing pads are required. This can be achieved if the process overlay is improved. To accomplish this, a lithography system must analyze and compensate for distortion errors caused by the repeated thermal cycling of the copper-clad laminate (CCL) panel and dielectric throughout the buildup process. Accurate metrology data is needed to generate an optimum alignment solution. However, this data is typically available after the lithography process is completed and the overlay of the vias to the RDL landing pad is measured. It is important to analyze this overlay data and feed corrections back to the stepper to compensate for the panel distortion of future panels.

Another area of concern involves the unique nature of the AICS process. For wafer-based devices, the active circuitry construction only happens on one side of the wafer. But for AICS, both the front-side and the backside of the panel will be processed. This significantly increases the risk of yield loss from defects caused by surface contamination. In addition, AICS has relatively few packages per panel. For example, a 510mm x 515mm AICS panel can only accommodate 16 packages (120mm x 120mm) compared to fan-out panel-level packaging (FOPLP), which could have over 2,300 packages. In other words, one defective package on an AICS could result in a 6.25% yield loss, whereas with FOPLP, one defective package may represent a 0.04% yield loss. As AICS package sizes increase to 150mm x 150mm, yield challenges are exacerbated: a single defective package failure results in an 11% yield loss.

Plating, dry film resist and buildup film lamination non-uniformity, RDL line defects, and more subtle buried defects, such as under-laminate bubbles and particles, can all contribute to yield loss. More stringent process control via metrology measurements and inspection after each critical step alerts manufacturers of a potential process excursion so that immediate corrective action can be taken. AICS manufacturing is a lengthy process and takes weeks to process both sides of the panel. As such, the real-time tracking of yield at every layer can help reduce the amount of time spent on processing defective substrates.

#### Conclusion

Advanced packaging is just one piece of the AI puzzle, but in this More Than Moore era, the back end of the process is more important than ever. In this article, we've outlined several key challenges facing the advanced packaging of AI devices, from measuring CD and identifying defects related to TSVs and microbumps to the real-time tracking of defective packages in the AICS production process. With the AI market driving current semiconductor industry growth, the solutions described here will become key pieces to completing the puzzle of how to meet the rapidly surging demand for AI packages.



Nobody Talks Nerdy Like We Do!

# Driving Into the Future: The Next Phase in Automotive Compute Package Adoption

By Prasad Dhond, Amkor Technology, Inc.

Automotive processors are rapidly adopting advanced process nodes. NXP announced the development of 5nm automotive processors in 2020 [1], Mobileye announced EyeQ Ultra using 5nm technology during CES 2022 [2], and TSMC announced its “Auto Early” 3nm processes in 2023 [3]. In the past, the automotive industry was slow to adopt the latest semiconductor technologies due to reliability concerns and lack of a compelling need. Not anymore.

The use of advanced processes necessitates the use of advanced packaging as seen in high-performance computing (HPC) and mobile applications because [4][5]:

1. While transistor density has skyrocketed, I/O density has not increased proportionally and is holding back chip size reductions.
2. Processors have heterogeneous, specialized blocks to support today's workloads.
3. Maximum chip sizes are limited by the slowdown of transistor scaling, photo reticle limits, and lower yields.
4. Cost-per-transistor improvements have slowed down with advanced nodes.
5. Off-package dynamic random-access memory (DRAM) throttles memory bandwidth.

These have been drivers for the use of advanced packages like fan-out in mobile and 2.5D/3D in HPC. In addition, these drivers are slowly but surely showing up in automotive compute units in a variety of automotive architectures as well (Figure 1).

Vehicle electrical/electronic (E/E) architectures have evolved from

100+ distributed electronic control units (ECUs) to 10+ domain control units (DCUs) [6]. The most recent architecture introduces zonal or zone ECUs that are clustered in physical locations in cars and connect to powerful central computing units for processing. These newer architectures improve the scalability, cost, and reliability of software-defined vehicles (SDVs) [7]. The processors in each of these architectures are more complex than those in the previous generation.

Multiple cameras, radar, lidar, ultrasonic sensors, and more feed data into the compute units. Processing and inferencing this data require specialized functional blocks on the processor. For example, the Tesla Full Self-Driving (FSD) HW 3.0 system-on-chip (SoC) has central processing units (CPUs), graphic processing units (GPUs), neural network processing units, Low-Power Double Data Rate 4 (LPDDR4) controllers and other functional blocks - all integrated on a single piece of silicon [8]. Similarly, Mobileye EyeQ6 has functional blocks of CPU clusters, accelerator clusters, GPUs, and an LPDDR5 interface [9].

As more functional blocks are introduced, the chip size and

complexity will continue to increase. Instead of a single, monolithic silicon chip, a chiplet approach with separate functional blocks allows intellectual property (IP) reuse along with optimal process nodes for each functional block [10]. Additionally, large, monolithic pieces of silicon built on advanced processes tend to have yield challenges which can also be overcome using chiplets.

Current advanced driver-assistance systems (ADAS) applications require a DRAM bandwidth of less than 60GB/s which can be supported with standard double data rate (DDR) and LPDDR solutions. However, ADAS Level 4 and Level 5 will need up to 1024 GB/s memory bandwidth which will require the use of solutions such as Graphic DDR (GDDR) or High Bandwidth Memory (HBM) [11][12].

Automotive processors have been using flip-chip ball grid array (FCBGA) packages since 2010. FCBGA has become the mainstay of several automotive SoCs such as EyeQ from Mobileye, Tesla FSD, and NVIDIA Drive. Consumer applications of FCBGA packaging started around 1995 [13], so it took more than 15 years for this package to be adopted by the automotive industry. Computing units in the form of multichip modules (MCMs)

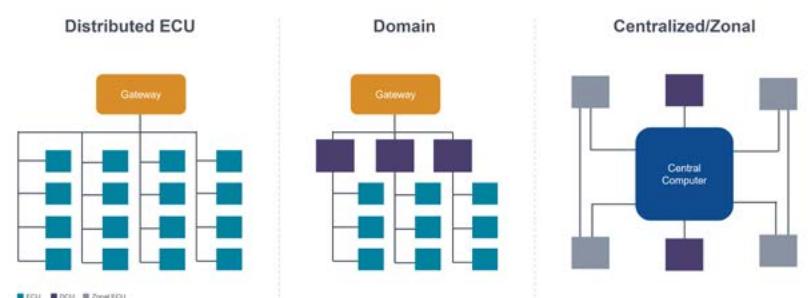


Figure 1. Vehicle E/E Architectures

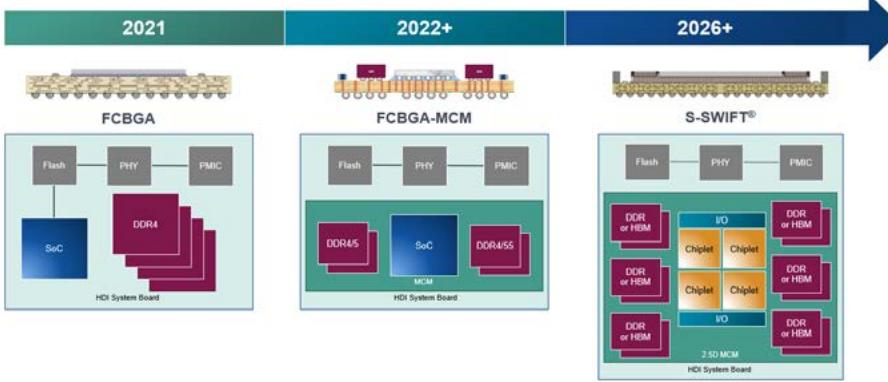


Figure 2. Automotive Compute Package Roadmap

or system-in-package (SiP) have also been in automotive use since the early 2010s for infotainment processors. The use of MCMs is likely to increase in automotive computing to enable components like the SoC, DRAM, and power management integrated circuits (PMIC) to communicate with each other without sending signals off-package.

As cars move to a central computing architecture, the SoCs will become more complex and run into size

and cost challenges. Splitting these SoCs into chiplets becomes a logical solution and packaging these chiplets using fan-out or 2.5D packages becomes necessary. Just as FCBGA and MCMs transitioned into automotive from non-automotive applications, so will fan-out and 2.5D packaging for automotive compute processors (Figure 2). The automotive industry is cautious but the abovementioned architecture changes are pushing faster adoption of advanced packages. Materials, processes, and factory controls

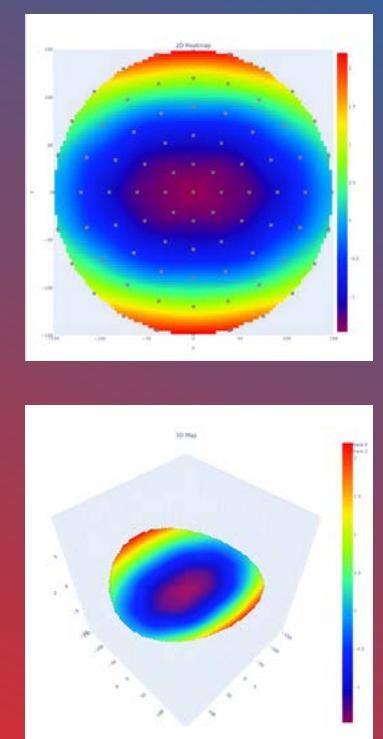
are key considerations for the successful qualification of these packages in automotive compute applications.

In summary, the automotive industry is adopting advanced semiconductor technologies, such as 5 nm and 3 nm processes, which require the use of advanced packaging due to limitations in I/O density, chip size reductions, and memory bandwidth. Processors in the latest vehicle E/E architectures are more complex and require specialized functional blocks to process data from multiple sensors. As cars move to the central computing architecture, the SoCs will become more complex and run into size and cost challenges. Splitting these SoCs into chiplets becomes a logical solution and packaging these chiplets using fan-out or 2.5D technology becomes necessary.

Continued on page 69

- Multi-function measurement platform that mitigates yield loss
- Generates an interactive 3D view of the wafer
- High throughput system with measurement in less than 1 minute

## Warpage Inspection System - Wave3000



# Leading The Charge to One Trillion Dollars

## A Conversation About Leadership with SEMI CEO Ajit Manocha

By Françoise von Trapp

For the past few years, we've heard semiconductor market analysts prognosticate that based on estimated demand, semiconductors have the potential to become a \$1Trillion industry in the next 7-10 years. This number is based on analysts' projections of driving markets including artificial intelligence (AI), electric and autonomous vehicles, 5G and 6G networks, high-performance computing, data centers... the list goes on.

The operative word here is "potential." Roadblocks like supply chain issues, sustainability goals, geopolitical issues, a global talent shortage, and an economic downturn are all impacting how and when we actually reach this goal. Make no mistake, the demand is there. But achieving it sustainably is going to take collaboration and strong leadership. As SEMI President and CEO, Ajit Manocha has been known to say, "No single CEO, no single company, no single country, can achieve everything we need to do to meet our 2030 goals of \$1T and Net Zero."

After interviewing Ajit for the 3D InCites Podcast and hearing him speak so passionately about the industry that he has served for over 40 years, I decided his personal journey was the story we wanted for the cover of the 2024 Yearbook.

So we sat down and started talking. With little prompting, Ajit shared anecdotes of his journey as a student of leadership, and how he implemented all the lessons he learned in each role he held as he climbed the executive ladder. In this article, he shares what it means to be a leader in the semiconductor industry over the past four decades, the lessons he's learned, and how one thing led to another to bring him to the pinnacle of his career as the head of the world's largest semiconductor association.

### Choosing the Semiconductor Path

To hear Ajit tell it, it seems like the semiconductor industry chose him, and not the other way around. In India, where he grew up, there were two professional paths that parents encouraged their children to pursue above all others: medicine and engineering. "And that's still the case today," he noted. Luckily, he was fascinated by science, technology, engineering, and math (STEM). "I was pretty strong in math, chemistry, and physics."

Majoring in Chemistry, Ajit completed his undergraduate and graduate studies in India. He moved to the U.S. for a research



Our interview took place at SEMI Headquarters in Milpitas, where a silicon ingot stands to represent the sand-to-microchips journey of semiconductor manufacturing.

position at Bell Labs, which was at the time (1980s) the most prestigious research institute in the world. As his first job out of university, Ajit says it was like hitting the jackpot. "I was told that my job is to serve mankind in the semiconductor technology arena," he recalls. And that's a job he took very, very seriously throughout his career.

At Bell Labs, he learned how semiconductors work, and how to use his chemistry degree to solve some critical challenges. He developed and patented a process using Nitrogen trifluoride (NF3) to replace fluorocarbon-based chemistry which solved a major problem with polymer deposition on wafers. "That gave me a lot of motivation," he said. "When I filed that first patent, it was like 'Wow! I'm an inventor now!' And it was a big deal." He remembers the thrill of filing those early patents, and the accolades that came along with it – coffee with the boss, a patent book, your name in the newspaper. He was hooked.

In those days, the key performance indicator (KPI) of Bell Labs was to produce one patent a day. As his patent filings started piling up, Ajit was promoted from a member of the technical staff in R&D to supervisor – which is the equivalent of VP of R&D today. He was now in charge of a research team, and his goal for that team was to set records for patent filings.

### Early Lessons in Leadership

A researcher at heart, Ajit pays attention to all the variables and makes assessments and decisions about what to do next. He is not so arrogant to think he knows everything about being a leader, just because he was promoted.

In fact, one of the earliest and most memorable lessons he learned was from, the head of HR at Bell Labs. He came to her for advice after discovering that despite his team's great success in filing more patents than any other department, they were not happy. When he asked one of them why, he told him, "These are all your ideas, not my ideas." When other members of the team confirmed this sentiment, Ajit was troubled. The HR lead's advice? Stop being a micromanager and give them a chance to work on their ideas.

He listened to her, and productivity and patent applications increased even more. This was a pivotal moment for Ajit when he learned the difference between being a boss and being a leader. And it guides him today.

### Climbing the Ladder of Leadership

Fixing complex problems is Ajit's superpower, and it's taken him around the world and up the ladder of success at some of the semiconductor industry's most renowned semiconductor companies.

When there was a disconnect between the lab and manufacturing when implementing processes developed at Bell Labs, Ajit requested a rotation in manufacturing to understand the other side of the story. So, they sent him to fix issues at the Madrid fab. There, he navigated cultural differences to better understand the Spanish work/life balance. This was the 90s and work/life balance was not a global initiative like it is today.

"In semiconductor manufacturing, there is no work/life balance, because fabs run 24/7 and customers expect timely delivery," he explained. Finding that alignment between business culture and the country's culture was a tightrope walk. Ajit said he wanted to respect their culture but also demanded productivity while they were on the job. He got his message across, because the fab became productive, even though the Spanish and European culture still demands work/life balance. "Instead of giving us more money, give us more days off," he said. "They want to enjoy life."

Ajit must have a million stories like this one, as his career path took him from fixing the fab in Madrid to managing the merger of AT&T Microelectronics and NCR microelectronics; advising on, and co-leading the spin-out of Philips Semiconductors (now NXP) from Philips; retiring and serving on multiple boards; coming out of retirement to serve as CEO of GlobalFoundries; and coming out of retirement AGAIN to lead SEMI as the semiconductor industry endeavors to find a sustainable path to \$1 Trillion.



## Ajit Manocha's 10 Guiding Principles of Leadership

Through it all, Ajit swears by 10 guiding principles of leadership that his team at Philips Semiconductors presented him while they were setting new records of success during his early years at the company. Garnered from two years of monthly all-hands meetings, these were his pearls of wisdom that they took away from the talks. He was quite touched to learn that they'd been paying such close attention. The goal of these guiding principles is to succeed by making customers even more successful.

1. Preach and practice: With the people, for the people, and by the people. Ajit says this is the most important principle and stems from what he learned early in his role as a lab supervisor.
2. Think of your job as your own business. You'll always give more and think differently when you're running your own business than if you're working for someone. As president and CEO of SEMI, Ajit has extended this principle to thinking of the entire semiconductor industry as his own business, and it shows.
3. If you are not part of the solution, then you are part of the problem. Ajit takes this one even further to say:
4. If your people are not part of the solution, then management is part of the problem. He advises managing people, not the issues.
5. Change people, or change people, until everyone is aligned to the common goal. Note the underlined emphasis. If people won't change to align, then they must be replaced with those who are aligned.
6. Make yourself redundant because that helps you develop your people. It might make you feel insecure, but in the end, it's healthier for the organization.
7. Market your people's contributions that lead to customers' success
8. Focus on the success, not just the good results.
9. Anticipate and manage the unknown. Anyone can manage what is known to them. Managing the unknown, such as the industry cycles, is very important for good leadership.
10. Remember, your future is in your own hands.

### Highlights and Key Takeaways

Ajit says that one of the highlights of his career was as CEO of GlobalFoundries, helping to establish a semiconductor ecosystem when GlobalFoundries was just a greenfield fab in Malta, NY. At the time, he was serving on President Obama's committee for advanced manufacturing, partnership, and communities. He recalls Obama's visit, when there was no ecosystem, and GlobalFoundries was just a greenfield fab in the boondocks of Malta, New York. He was struggling to find the workforce to fill the fab, and Obama said to him, we're investing \$10 billion, so fix it.

GlobalFoundries hired around 350 veterans and trained them to become technicians. And that was the beginning of a program for hiring veterans. Today, at SEMI he's charged SEMI Foundation with the task of developing a VetWorks Initiative as one lever to address the global semiconductor talent shortage.



Ajit dressed as Sinterklaas for his Dutch coworkers at Christmas time.

# Accelerating heterogeneous integration through faster 3D insights

## ZEISS Advanced 3D X-ray Microscopes



These days, Ajit is most passionate about the PFAS issue, which involves "forever" chemicals that are slated to be phased out from use in the coming years. Finding alternatives to replace these pervasive materials is a bigger challenge than wafer processing issues he dealt with early in his career. To address this, he brought together policymakers from multiple regions to discuss industry issues with top executives at a first-of-its-kind summit held during the International Trade Partners Conference (ITPC) in October.

This event demonstrated Ajit's recognition of the value of respecting local cultures and keeping close ties with governments to minimize surprises and avoid exploitation. And while the PFAS issue represents a challenge that "no single CEO, no single company, no single country" can address, if anyone can bring them together to make it happen, Ajit can.

By following his own guiding principles, Ajit's career path has led him around the world and made him a much sought-after consultant, especially when it comes to forming collaborations. He understands the importance of building an ecosystem to support fabs. He realizes the importance of establishing a solid business culture while not disrupting a country's culture.

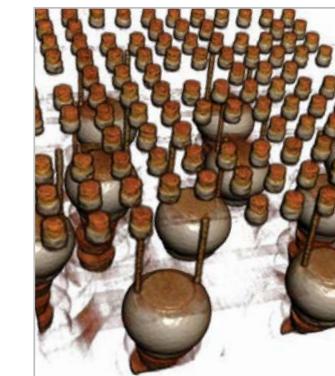
Could there be a more qualified individual to lead the industry to sustainably achieving its \$1Trillion goal? He's too humble to admit it. But I'd put my money on him.

### Achieve High-contrast, High-resolution Images Non-destructively



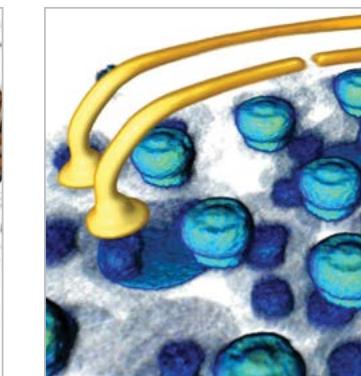
Visualize structures and defects within intact 15-die DRAM package

### Enable Fast, High-resolution Imaging with AI



Improve failure analysis speed by 4X on 2.5D interposer package

### Guide FIB Sample Preparation with Correlative Workflow



Prepare XRM-guided site-specific FIB cross section of PoP device



Seeing beyond

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# Five Workflows for Tackling Heterogeneous Integration of Chiplets for 2.5D/3D

Kevin Rinebold, Siemens EDA

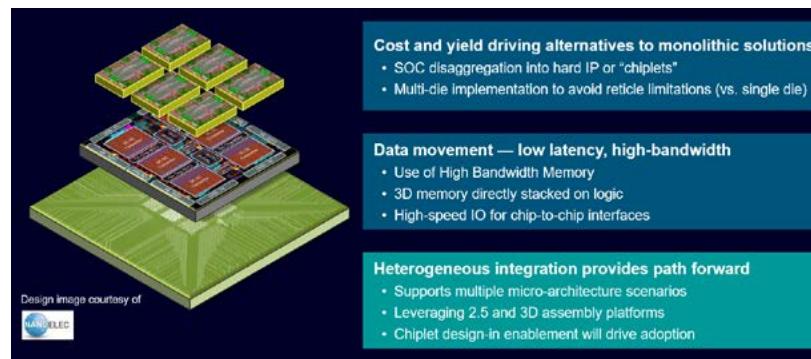


Figure 1: Chiplets answer semiconductor scaling challenges.

Keeping pace with Moore's law continues to be challenging and is driving the adoption of innovative packaging technologies that support continued system scaling while doing so at lower costs than comparable monolithic devices.

These packaging technologies disaggregate what would typically be a homogenous, monolithic device — like an ASIC or system-on-chip (SoC) — into discrete, unpackaged dies, known as chiplets, specifically designed and optimized for operation within a package in conjunction with other chiplets (Figure 1). This is also referred to as heterogeneous integration (HI), where multiple dies or chiplets are integrated into a system-in-package (SiP) design.

Heterogeneously integrated SiP devices offer considerable benefits, including higher performance, lower power usage, smaller area, lower cost, and faster time to market. However, thus far they are designed and produced by only a small number of advanced users. Broad industry proliferation will require a standardization of chiplet models and die-to-die connectivity IP—efforts currently underway—supported by new workflows.

This article will focus on five workflows that are essential for planning, implementing, verifying, and co-designing heterogeneous designs (Figure 2).

1. Architectural planning and analysis
2. Physical design planning and analysis
3. Design analysis
4. Reliability analysis
5. Test planning and validation

Now let's look at the five workflows themselves in a little more detail.

## Architectural Planning and Analysis

The architectural planning and analysis workflow enables system and RTL designers to rapidly explore and capture viable design architectures leveraging three key inputs:

- The chiplet components and corresponding design kits
- Standard high-speed protocols for internal die-to-die interfaces within the package
- External chip-to-chip interfaces between the SiP package and other chips within the system at the PCB level

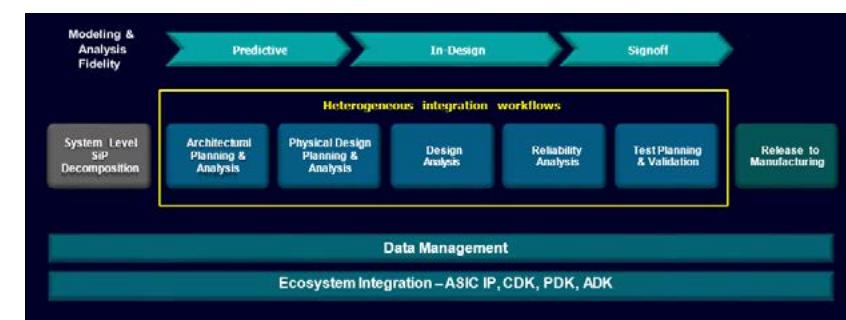


Figure 2. Heterogeneous integration workflows.

In-design modeling further qualifies a design as more content and details become available during implementation. The objective is to identify and resolve issues while corrective action is still relatively easy and inexpensive. These issues are typically related to power, thermal, signal integrity, process rules, or even mechanical integration.

The last step is the final signoff of the completed design before release to manufacturing. Because HI designs include a wide range of multi-domain design content and IP, comprehensive data management support throughout all five workflows is required.

Now let's look at the five workflows themselves in a little more detail.

These high-speed interfaces can be captured using a library of generic connectivity IP models and then mapped to alternate vendor-specific and technology-specific connectivity IPs. This enables the system designer to assess the power, performance, area, and cost attributes of various scenarios against the system requirements.

In this way, predictive modeling helps engineers to hone in on the optimal micro-architecture through the identification of a finite set of scenarios, or micro-architectures, and the exploration of multiple configurations, and partitioning scenarios.

## Physical Design Planning and Analysis

Once an optimal SiP architecture is identified, detailed design can begin, including physical planning, implementation, and analysis.

The physical design planning and analysis workflow applies to both interposers and package substrates. It encompasses package floor

planning, IO planning, power delivery, substrate route feasibility, and netlist optimization, along with the corresponding checks, such as LVS and LEC.

Predictive modeling is used during floorplanning and implementation to continuously qualify the design, which ultimately streamlines the design process. As detailed design structures, like power planes, get implemented, the modeling fidelity and quality of results will improve.

As co-design of one or more custom chiplets is fundamental, tight collaboration between the silicon and package design teams must be fully supported. This means establishing robust multi-domain design data management along with comprehensive engineering change order support to facilitate the exchange of data between teams and disciplines.

## Design Analysis

The design analysis workflow incorporates extraction and simulation tools that support

analysis of SiP signal and power integrity, static and dynamic IR drop, electromigration, and timing.

Traditional signal integrity techniques can be used to simulate the high-speed interfaces. Static timing analysis is required for the low-speed signals and the test and control type connections.

The power integrity approach taken must be adapted to account for multi-chiplet scenarios. These structures require detailed parasitic extraction that supports both silicon and organic substrates as well as combined SiP and die level extraction for IR drop and electromagnetic analysis.

## Reliability Analysis

Two key areas that require extensive reliability analysis are thermal and mechanical stress. Given the proximity of devices in HI designs, there's a high likelihood of some type of chip-to-chip or chip-to-package interaction. Therefore, thermal coupling can be a big concern.

**Continued on page 70**



S T R A T E D G E

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# 2024 3D InCites Awards Finalists



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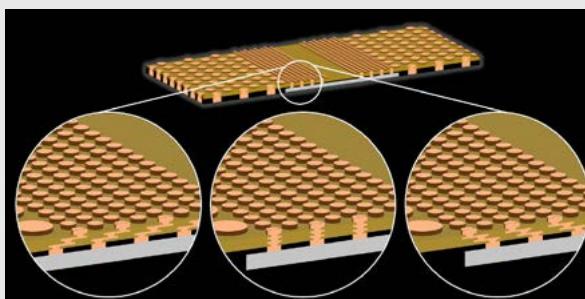


## Technology Enablement Awards

### DECA

The semiconductor industry is transitioning from silicon interposers to molded fan-out interposers with embedded bridge die for progressively larger devices. As highlighted in TSMC's keynote at IMAPS San Diego in October '23, precisely aligning embedded bridge dies presents a substantial manufacturing challenge that leads to potential risk of yield loss, particularly as devices become more intricate.

In response to this manufacturing challenge, DECA has unveiled a groundbreaking solution known as Adaptive Pad Stacks. This innovation signifies a significant leap forward, delivering an order-of-magnitude increase in the allowable die shift for embedded bridge die in molded fan-out interposers. The resulting enhancement in manufacturing tolerance not only safeguards against yield losses but also facilitates the highest density interconnect on more complex devices, including cutting-edge AI processor applications. When integrated

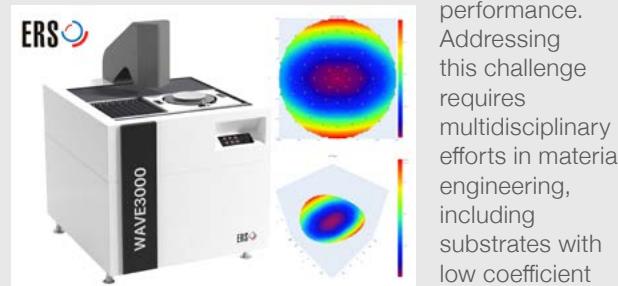


Adaptive Pad Stacks™ increase manufacturing process windows by 10X, facilitating the highest density interconnect for more complex devices, including cutting-edge AI processor applications.

with proven technologies such as Adaptive Alignment, Adaptive Routing, and Adaptive Metal Fill, Adaptive Pad Stacks provides a robust and comprehensive solution for foundries, OSATs, IDMs, and other industry players involved in designing and producing the most advanced HI chiplet assemblies of the future.

### ERS Electronic GmbH

Wafer and package warpages pose a significant challenge for the widespread adoption of HI, 3D HI, and Chiplet-based architectures. Thermal mismatch among different materials exacerbates this issue, potentially leading to misalignment of interconnects, reduced bonding efficiency, and long-term reliability concerns. Even minimal warpages in these advanced architectures can result in signal integrity issues and degraded



The ERS Wave3000 is a specialized warpage measurement system that is seamlessly integrated into various manufacturing line steps.

(CTE), underfill materials, process optimization, and advanced metrology tools for real-time monitoring during manufacturing.

To address wafer and package warpage, ERS Electronic GmbH developed the Warpage Measurement System Wave3000. This in-line metrology system accurately measures wafer warpage using advanced optical sensors, identifying risks before proceeding to subsequent processing steps. The Wave3000 can be integrated at various points in the manufacturing line, ensuring continuous monitoring and mitigation, to address warpage caused by integrating multiple materials with varying CTE. With its data-driven approach, the system provides crucial information ahead of time, enabling dynamic adjustments to process parameters and preventing the risk of sending warped wafers that subsequent machines may struggle to handle, ensuring mass production and commercial viability of HI, 3DHI, and Chiplets.

### LPKF Laser & Electronics SE – Laser-Induced Deep Etching



Roman Ostholt, Managing Director of the Electronics business unit at LPKF, discusses the different building blocks (TGV's, blind vias, cavities, through cuttings) that we can manufacture with the LIDE technology and how to combine them for a advanced packaging application.

Glass substrates are becoming a viable alternative to silicon for HI, 3DHI, and chiplets. However, there are challenges with cost-effectively achieving precise

and reliable through-glass vias (TGVs) and other microstructures using traditional drilling methods. Fabricating high-quality, high-density, and small-diameter TGV patterns in glass, without causing damage or stress, is paramount to realizing optimal device performance, achieving miniaturization, and ensuring cost efficiency and yield.

To address this challenge, LPKF Laser and Electronics developed its Laser-induced deep etching (LIDE) technology. Using a non-ablative, single-pulse laser-based process, it's possible to achieve high aspect ratio, high-density TGV arrays without stress or microcracks. LIDE is ultra-fast and can create multiple structures in one step. It's also compatible with a range of glass types, including thin and ultra-thin substrates.

LIDE technology is said to be highly scalable and suitable for mass production. Its promise of rapidly and reliably producing high-quality glass microstructures positions LPKF as a key enabler in the commercialization and manufacturing of next-generation HI, 3DHI, and chiplet-based devices.

decision-making with low power and low latency, promising breakthroughs in chips-first and chips-last packaging and on-wafer extended integration.

Multibeam's technology accelerates time-to-market for multi-die packages and overcomes throughput limitations. Its scalable modular architecture allows for seamless transitions from pilot to production. Its adaptable and extendable patterning capabilities and the ability to customize substrates and implement design changes without masks position this technology to drive advancements in silicon integration for future generations.



The World's First High Productivity E-Beam Litho Systems—capable of 3D litho, adaptable patterning, and full-wafer deep sub-micron patterning.



## PulseForge, Inc.

Fabricating 3D ICs involves stacking thinned silicon (Si) wafers and vertically interconnecting them using through-silicon vias (TSV). To handle thinned Si wafers, temporary bonding to a rigid carrier is required before thinning. The crucial step of wafer debonding, separating the thinned wafer from the carrier, is typically done using chemical solvents, mechanical means, or heating the adhesive. Laser-assisted wafer debonding is an attractive alternative, leveraging optical energy to promote adhesion loss at room temperature. However, challenges like beam width limitations necessitate exploring alternative high-throughput debonding techniques.

Photonic Debonding (PDB) utilizes high-intensity light pulses and a proprietary inorganic light-absorbing layer to separate temporarily bonded wafer pairs efficiently. This technology offers a cost-effective alternative to traditional laser techniques, providing benefits such as lower processing costs, minimal thermal impact, reduced mechanical strain, and ash-free debonding. Operating at room temperature, PDB is particularly advantageous for advanced packaging applications, enabling efficient debonding of ultra-thin wafers during back-end-of-line processing with increased final device yield.

To bring PDB to market quickly, PulseForge formed strategic partnerships with material suppliers and

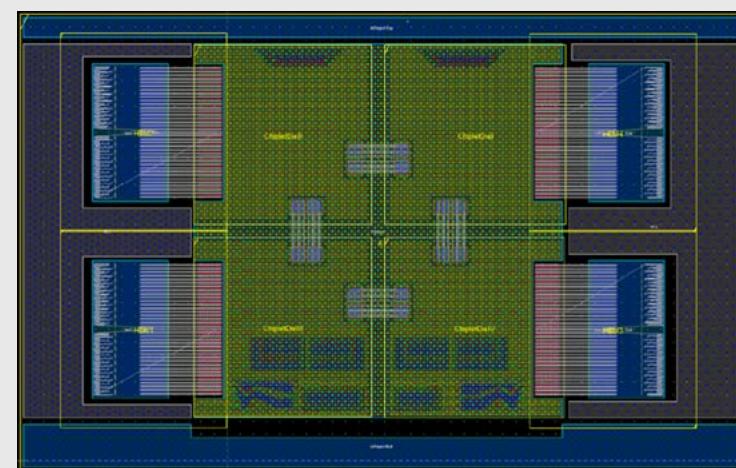


PulseForge PD300SA enables photonic debonding through high-intensity light pulses and proprietary light-absorbing layer-coated carriers.

integrators in the temporary bonding/debonding infrastructure. This collaborative approach not only opens new markets and introduces the technology to customers but also validates it and gains support from multiple stakeholders. The company offers a three-tiered approach: a flexible R&D tool for fundamental research, a semi-automated debond tool for limited production, and a fully automated debond tool for fabs as a drop-in replacement for existing equipment. An extensive patent portfolio has also been developed around the equipment and the PDB process.

## Siemens DISW

The semiconductor industry faces a challenge in adapting to the megatrend of chiplet integration for high-performance computing. Early design planning involves optimizing pin layouts for power, performance, and area, particularly in high pin count ASICs/FPGAs. These are broken down into smaller blocks, forming the complete floor plan over time. Hierarchy in design helps manage complexity by breaking structures into smaller building blocks. Parameterized representation is crucial, especially in die-to-die signal interfaces and power distribution networks within IC packaging.



A design with 4 logic processor chiplets connected to 4 HBM 1.0 memory stacks. The 4 processor chiplets were disaggregated from a monolithic SoC architecture using Hierarchical Device Planning with parameterized pin regions using 4 levels of device hierarchy and are interconnected using UCIe interfaces.

Siemens uses hierarchical device modeling methods to enhance its package prototyping and planning design tool, Xpedition Substrate Integrator (XSI). This innovative set of functions and capabilities facilitates quick and comprehensive updates to design structures consisting of hierarchical building blocks or parameterized pin regions. In contrast to non-graphical IC package floor-planning flows that rely on macro-driven spreadsheets, Siemens' approach minimizes time consumption and reduces the risk of errors during design updates.

While non-graphical floor-planning flows can generate an initial draft, keeping up with changes needed for early design analysis could be more practical. Demonstrating the efficiency of an HBM die-to-die building block with parameterized pin regions, this approach enables quick and efficient package design creation. Notably, effective hierarchy incorporation achieves iterative updates in minutes or seconds. Integrating hierarchical device planning with parameterized pin regions in the XSI design tool offers a revolutionary methodology, significantly reducing design cycle time to meet performance, power, area, and cost (PPAC) goals.

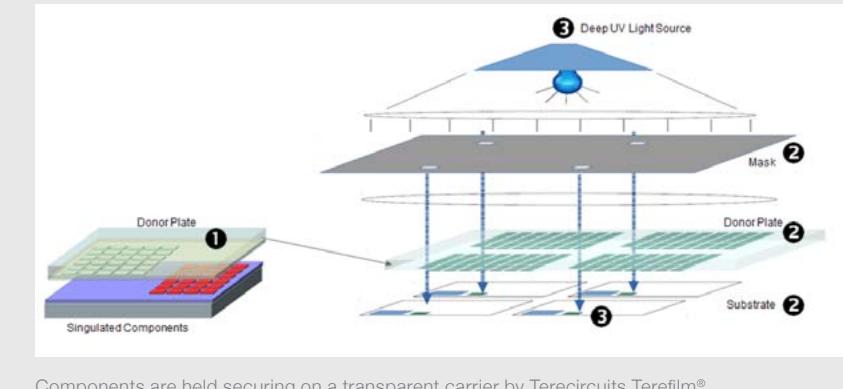
## Terecircuits

Current advanced packaging techniques, such as 3D stacking, HI, and die-on-wafer, introduce complexity and additional process steps, impacting yield and slowing down throughput. To overcome these challenges and unlock the potential of advanced packaging and assembly for complex devices, Terecircuits founders envision their foundational chemistry and processes becoming the industry standard, particularly for semiconductor and display back-end manufacturing.

Traditional pick-and-place tools struggle with assembling large numbers of microscopic components, hindering the development of next-gen displays, wearables, and medical devices.

Terecircuits addresses this challenge by proposing a shift from slow and inefficient mechanical processes to a fast, controllable chemical approach.

Terecircuits' efficient Laser-Induced Forward Transfer (LIFT) technique, powered by a new photopolymer class, delivers a cost-effective, high-yielding 10-10,000x



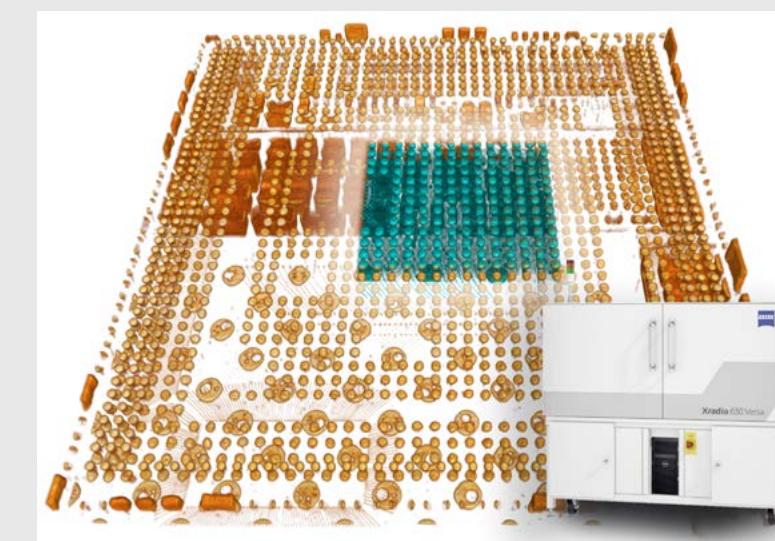
Components are held securing on a transparent carrier by Terecircuits Terefilm® photopolymer. A scanning laser cleanly releases components by individual die, row, or column for gentle assembly of small, thin, and fragile assembly without pick & place.

throughput improvement. The applications span from mass transferring MicroLEDs for displays to the non-destructive transfer of delicate materials like Silicon Carbide (SiC), and stress-free assembly of thinned die for 3D stacking and flexible hybrid electronics.

Drawing inspiration from the semiconductor industry's success in using light and chemistry for modern integrated circuits, Terecircuits aims to revolutionize the \$200 billion assembly and packaging industry, offering a radical solution for assembling individual microscopic components efficiently.

## ZEISS

Complexities in 3D HI architectures are slowing down traditional package analysis, impacting success rates and extending development cycles. The limitations of X-ray microscopes (XRM) with field of view (FOV) constraints make fault isolation challenging in large IC packages, resulting in a time-consuming imaging process.



Xradia 630 Versa and large field of view image of Integrated Fan-out Package reconstructed with ZEISS DeepScout

ZEISS revolutionizes 3D X-ray microscopy with AI-powered solutions for non-destructive imaging. DeepRecon Pro enhances imaging in advanced 3D packages, providing superior quality and over 4x faster data acquisition. Meanwhile, DeepScout, also AI-enabled, achieves up to 5x higher resolution for extensive FOV imaging through a deep-learning algorithm.

ZEISS's AI-powered DeepRecon Pro enhances thermocompression bonding (TCB) processes in 2.5 and 3D packages, reducing scan times for assessing alignments and accelerating process development cycles. DeepScout extends high-resolution 3D X-ray imaging benefits to reliability testing, construction analysis, and reverse engineering applications.

Congratulations to all our Technology Enablement Award Finalists! After a final round of questions, winners will be selected and announced on February 5, 2024. The 3D InCites Awards Ceremony takes place on March 21, 2024, following the morning keynote session at the IMAPS Device Packaging Conference.



## Sustainability Award

The 3D InCites Sustainability Award recognizes a company in the semiconductor and microelectronics industries that demonstrates best practices in support of sustainable semiconductor and microelectronics manufacturing.

Dean Freeman, Chief Analyst, Freeman Technology and Market Advisors, Julia Goldstein, Owner, JLFG Communications and Author of Material Value, and Mousumi Bhat, Ph.D., VP of Sustainability Programs comprise this year's selection committee. They reviewed applications submitted that answered questions about water consumption, recycling, and wastewater; renewable energy usage; actions to reduce waste generated; how they measure Scopes 1 and 3 emissions; plans for carbon neutrality, and environmental sustainability initiatives.

This year's finalists are Namics Technologies and Brewer Science. The finalists will respond to another round of questions about employee engagement, new programs being ramped up, and goals for 2030 and 2040. The winner will be announced on February 5, and the award presented at the IMAPS DPC on March 21.

### Brewer Science

Brewer Science has implemented several initiatives to enhance environmental sustainability. In 2022, the company replaced water chiller/tower systems, resulting in significant electrical savings and reduced water consumption. Upgrades to deionized water systems and water softeners contributed to monthly water savings. Brewer Science is committed to 100% waste diversion from landfills, achieving GreenCircle Certified Zero Waste to Landfill for the eighth consecutive year. The company measures Scope 1 and 2 GHG emissions per product volume and plans to report Scope 3 GHG emissions in the 2024 Impact Report.

The company's goal is to achieve a net-zero carbon footprint by 2050 through green building principles, renewable energy support, and efficient practices. Recent sustainability successes include consistent energy



Brewer Science employees participated in a street cleanup event.

consumption despite production increases, installation of efficient HVAC and lighting systems, and the use of a closed-loop geothermal system at the company's Vichy facility. Brewer Science purchases wind energy at its Rolla location through renewable energy credits, covering over 100% of electricity consumption in 2022.

### NAMICS Technologies, Inc.

NAMICS is committed to preventing water contamination and employs strict control and treatment measures for wastewater. The company recycles wastewater byproducts and products from various processes, promoting sustainability. Recently completing the construction of a carbon-neutral headquarters, NAMICS plans to install a solar canopy over its parking lot for increased reliance on renewable energy. The company has invested in two solar farm locations, contributing to substantial annual power generation and carbon dioxide emission reductions.

NAMICS is actively reducing waste and promoting sustainability through initiatives such as optimizing shipping boxes and pallets, resulting in reduced cardboard and Styrofoam use. They've transitioned to 100% recycled dry ice for shipments. Greenhouse gas emissions are measured at each facility. The recent construction of a carbon-neutral headquarters

demonstrates their commitment, with ongoing investments aimed at achieving a carbon-neutral company by 2050. Other initiatives include converting cooling pumps to inverters, using film-on-glass surfaces to reduce energy consumption, and transitioning to electric vehicles. Overall, the company prioritizes comprehensive sustainability measures, from packaging optimization to energy-efficient infrastructure.



NAMICS employees engage in neighborhood cleanup around the company's corporate headquarters in Japan.

## Adele Hars Award for DEI

The Adele Hars Award for Diversity, Equity, and Inclusion recognizes a company in the semiconductor and microelectronics industries that demonstrates best practices to provide a workplace where diversity, equity, inclusion, and belonging are paramount. Formerly known as the SemiSister Award for DEI, the award was rechristened for 2024 in loving memory of our SemiSister, Adele Hars, a well-known semiconductor industry journalist who lost her 20-year battle with breast cancer on July 23, 2023.

Adele was kind, thoughtful, and incisive. She didn't hesitate to share her ideas on the topic of DEI. She also kept us all in check when we got too righteous about our cause. "This is an industry issue about which Adele felt very strongly, and in her subtle way she always labored to promote DEI in the community she covered," said her husband, Emery Davis.

This year's selection committee, Margaret Kindling, SEMI Foundation; Veronique Pequignat, Invest in Grenoble Alpes; and Joanne Itow, SEMICO Research, reviewed applications that answered questions about building an inclusive workplace culture and environment, diversity solutions in hiring, practices concerning social justice and systemic racism, fair access to career advancement, involvement of the executive leadership, and the overall company mindset.

This year's finalists are Cadence and ERS Electronic GmbH. Each company will respond to a tiebreaker question: How does your executive leadership, especially your CEO, promote DEIB to peers to affect positive industry change? Like all the others, the winner will be announced on February 5, and the award presented at the IMAPS DPC on March 19.

### Cadence

Cadence prioritizes a culture of trust and collaboration, emphasizing inclusivity to address gender and racial disparities in the tech industry. Its DEI journey began over nine years ago, focusing on women in technology initially and expanded to include various underrepresented groups in 2020. Regular events featuring thought leaders promote awareness of crucial DEI topics. Cadence measures global employee engagement through surveys, using feedback to ensure an inclusive workplace. The company participates in the Great Transformation initiative to further progress in gender equity, experimenting with new initiatives and collaborative efforts to positively impact the experience of women at Cadence.

Cadence has implemented a comprehensive DEI approach across its organization. The company prioritizes creating a sense of belonging for its employees, emphasizing a people-first culture that values individual strengths and talents. They actively monitor workforce diversity and collaborate with national engineering organizations and colleges to engage with diverse communities. The company supports a returnship program to bring talented employees back into the workforce, especially women and caregivers who left to support their families. It also offers referral bonuses for underrepresented candidates and invests in scholarships for underrepresented students in technology.

In addressing equity, Cadence provides unconscious bias training, regularly reviews compensation



"Women across Cadence joined together and celebrated their achievements at the Global Cadence Women Conference."

practices, and has achieved global salary pay parity. The company's "Words Matter Initiative" focuses on respectful language, and it contributes to various organizations promoting STEM diversity. Additionally, Cadence launched a \$50 million Racial Equity Fund to address racial wealth inequities, investing in projects that support underserved communities. The company is committed to promoting social justice and fostering diversity throughout its value chain, including supplier programs.

Cadence promotes fair access to talent development and career growth through initiatives like the Advanced Leadership Program for top women, Black, and



Latinx talent. The IMPACT mentorship program allows employees to choose mentors aligned with their career goals. CEO Anirudh Devgan signed the Global Semiconductor Alliance's Women's Leadership CEO Pledge, showcasing a commitment to gender diversity. Cadence fosters a learning culture, with employees completing 25 hours of training annually, utilizing resources like Harvard University's ManageMentor and LinkedIn Learning. The company also offers up to \$5,000 in annual tuition reimbursement for relevant fields.

Cadence prioritizes a high-performing, inclusive culture integral to the CEO's success pillars. Leadership's role is emphasized through a unique compensation incentive, tying 20% of senior leaders' bonuses to DEI and inclusion goals. Each of the eight inclusion groups has

an Executive Sponsor for representation and support among executive peers.

Cadence fosters a purpose-driven mindset, emphasizing its employees' impact on technology, communities, and the environment. The company aligns its ESG efforts with community, environment, technology, and workforce, reflecting a commitment to innovation and inclusivity. The company participates in the Pledge 1% alliance and encourages employee involvement in charitable activities. Employees are granted 40 hours of paid volunteer time annually, contributing to a Season of Giving campaign and collaborations with organizations supporting diverse communities. Cadence's Inclusion Groups nominate organizations for donations, furthering its commitment to social impact and diversity.

#### ERS electronic GmbH

ERS prioritizes building an inclusive workplace culture centered on values like fairness, respect, appreciation, and belonging. The company fosters an open and safe environment, encouraging growth and empowerment. With a diverse team from 20 countries, ERS emphasizes the strength of diversity. Open discussions, valuing diverse perspectives, and ensuring every voice is heard contribute to a culture that acknowledges imperfections, values inclusivity, and is committed to continuous growth.

The company prioritizes transparency and values alignment in its hiring process. Celebrating cultural festivities and bilingual communication fosters team uniqueness. Remote work during holiday visits accommodates diverse needs. Equal opportunities in career planning, emphasizing individual strengths, contribute to building a diverse, inclusive, and empowering workplace.

ERS appointed an Equal Opportunities Officer in 2020 to ensure equal career opportunities and salaries, conducting regular assessments of gender and managerial quotas. A reporting mechanism for misconduct is in place, aligned with the EU Whistleblowing Directive. Signing the Diversity Charter reflects a commitment to recognizing and addressing diversity positively.

ERS has open communication, tailored talent development, and a dynamic personnel development concept to guide fair access.

Aligned with ISO9001, structured skill development is facilitated by a qualification matrix. The HR

department, engaging closely with teams and individuals, supports career advancement. Top management ensures DEI integration by maintaining a diverse Senior Management Team, reflecting a commitment to principles in decision-making. This effort permeates the entire organization, fostering an inclusive environment for diverse perspectives and employee thriving.

ERS has a robust purpose-driven mindset that is actively cultivated among employees, instilling a strong commitment to community support. The organization prioritizes local suppliers for manufacturing, contributing to the growth of the local economy. Sustainability is integral to corporate culture, with employees actively involved in reducing the environmental footprint. ERS extends its impact by sponsoring sports communities and supporting local organizations, demonstrating a collaborative approach with the city council to contribute to community growth through local recruitment.



ERS is proud of having a diverse team consisting of more than 20 different nationalities.

## Best Place to Work

### Megatech Ltd.

Working in the semiconductor and microelectronics industry means being at the heart of technological innovation and digital transformation. At Megatech, this dynamic is doubly stimulating. Megatech offers employees a unique and stimulating experience. As a distributor, the company provides opportunities to collaborate with diverse companies, technologies, and industry experts, keeping employees at the forefront of technological developments. Beyond distribution, Megatech engages in its product lines, allowing

employees to participate in design and manufacturing projects, fostering skill diversification. The corporate culture emphasizes constant expansion and innovation, evident in the opening of new offices in Dublin and Leipzig. This growth translates into new career opportunities and strengthens Megatech's position in the dynamic semiconductor industry. Overall, Megatech is not just a workplace; it's a platform for professional fulfillment in a cutting-edge sector of modern industry.

### Moov Technologies

Moov, a key player in the semiconductor equipment marketplace, is an outstanding workplace in Phoenix's thriving semiconductor hub. With offices in Tempe, AZ, Austin, TX, and Taipei, Moov has created 100+ tech jobs. The company offers enticing benefits, promotes internal

growth, and has earned recognition for its workplace excellence. In the community, Moov actively supports nonprofits like Feed My Children and participates in local tree-planting initiatives, showcasing its commitment to both its employees and the community.

### Nhanced Semiconductors

Nhanced Semiconductors, Inc. (NSI) is an exceptional workplace where employees actively contribute to cutting-edge science and collaborative problem-solving. The company promotes professional growth through mentorship and specialized training, offering above-average salaries, comprehensive benefits, and a generous paid time off policy. With locations in

Batavia, Illinois, Odon, Indiana, and Morrisville, North Carolina, NSI provides a rewarding work environment and supports employees' personal and professional development. The company's diverse and talented workforce is dedicated to building a culture of collaboration and contributing to the growth of the semiconductor industry.

### Onto Innovation

Onto Innovation is an exceptional workplace, promoting employee well-being and technological innovation through core values like passion and collaboration. With over 1,500 global employees, the company emphasizes a tight-knit community of innovators, often co-locating offices with certified cleanrooms for hands-on collaboration. Employees enjoy a comprehensive benefits package, profit-sharing, and discounted stock options. Onto fosters a sense of importance,

belonging, and value through relationship building, extensive learning programs, and internal career advancement opportunities with ethical hiring practices. As a Responsible Business Alliance member, Onto adheres to high standards, ensuring employee safety and supporting community outreach through regular volunteer opportunities via its employee-led RISE program.

### Plasma-Therm

Plasma-Therm offers an exciting, collaborative work environment that values innovation. Its competitive benefits program includes HSA/FSA contributions, 401K matches, and support for education. The company prioritizes work/life balance with hybrid positions and

generous paid time off. Our transparent culture and regular recognition make Plasma-Therm a fantastic workplace. Located in a beautiful area with sandy beaches, our headquarters is the best place to work.

# EV Group: More than 40 Years of Growth Fueled by 3D/Heterogeneous Integration

By Paul Lindner, EV Group

For decades, the ability to power, performance, area, and cost (PPAC) in semiconductor manufacturing had been largely driven by 2D design rule shrinks enabled through advances in lithography. In recent years, however, the rising costs and complexity associated with 2D shrinks have made it increasingly difficult to continue PPAC scaling on lithography advances alone. Indeed, many industry observers have noted this as a sign that Moore's Law – the prediction that the number of transistors on an integrated circuit would double every other year – is either slowing down or is well and truly dead.

The reality is more nuanced. While it is true that the constant pace of rising transistor counts on monolithic 2D semiconductors has slowed down, the industry has continued to successfully scale the PPAC metric by turning to 3D vertical stacking and heterogeneous integration – the manufacturing, assembly, and packaging of multiple different components and dies into a single device or package. 3D and heterogeneous integration (HI) are enabling high-bandwidth interconnects in advanced

packaging to achieve overall system performance gains. As a result, they have become a crucial driver for AI, autonomous driving, and other high-performance computing applications. This is not to say that 2D transistor scaling via lithography

is not important. Rather, 3D/HI is stepping into the spotlight and sharing the stage with lithographic scaling as equal partners in driving performance improvements on new semiconductor device generations.

Since EV Group's founding more than 40 years ago, our vision has been steadfast in "being the first in exploring new techniques and serving next-generation applications of micro- and nanofabrication technologies". Our founders DI Erich and Aya Maria Thallner recognized from the beginning that semiconductor innovation requires a holistic approach – from

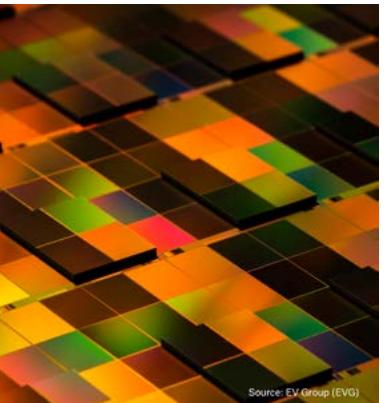


Figure 1: Chiplet integration by collective die-to-wafer hybrid bonding.

the integration of new materials and material combinations to the integration of different layers, components, and device types. As a result, EVG has maintained a strong level of investment in our products and infrastructure over the years to pioneer advances in heterogeneous integration and wafer-level packaging. This has led to many industry firsts in wafer bonding, lithography, and metrology technology (see Sidebar article).

It's no surprise that the increasing importance of 3D/HI in driving semiconductor innovation has coincided with an extended period of particularly strong growth at EVG. While demand has been on the rise across all of our major product areas, it has been particularly strong for our hybrid bonding solutions. The adoption of newer packaging technologies – from 2.5D to 3D system-in-chip (SiC) to 3D system-on-chip (SoC) – with tighter and tighter pitch requirements to support higher bandwidth needs are in turn fueling the need for new and different hybrid bonding techniques (Figure 1).

In addition to our strong R&D investments annually to develop new and innovative wafer bonding and other 3D/heterogeneous integration process solutions, EVG has significantly grown its headcount, process development, and production infrastructure to support

our customers' rapid growth and help them accelerate the deployment of their new products.

From our first manufacturing and assembly buildings at our headquarters, EVG has achieved consistent solid growth, with a surge in growth over the past few years. In 2018, EVG broke ground on our new Manufacturing III building near the River Inn, which doubled the floor space for the final assembly of EVG systems. We had the distinct pleasure of inviting the Queen of 3D herself, Françoise von Trapp, out to survey the site of our new building (Figure 2), which was completed in 2019. From there, our growth has continued at a strong pace to meet the ever-growing demands of our global customer base for our industry-leading process solutions.

EVG opened our Manufacturing IV facility at the end of last year and we have just completed and opened our Manufacturing V facility, which serves as the manufacturing department for EVG product components. The ultra-modern facility is fully air-conditioned with humidification and dehumidification systems and features 200 m<sup>2</sup> of window area offering lots of natural sunlight in addition to LED lighting throughout. In addition, it is ergonomically designed so that no objects need to be lifted by hand. Hydraulic lift platforms have been built into the floor to raise equipment modules and systems so that production workers can install additional components at eye level instead of having to bend down. Indoor cranes and other mechanisms are used to lift systems, components, and other objects for transportation to other halls and facilities.

In parallel, our existing Manufacturing II building has been converted to offer nine new test rooms for the final assembly of EVG's high-precision systems, as well as for technical source inspection of the systems by EVG's customers. As a result, EVG's headquarters today include a total of 62,000 m<sup>2</sup> of plant area, including more than 8,100 m<sup>2</sup> of production space, nearly 2,800 m<sup>2</sup> of test room space, and more than 9,500 m<sup>2</sup> of warehouse space. Manufacturing VI, EVG's next phase of expansion provides for an additional 1,400 m<sup>2</sup>

of production and an equal amount of warehouse space, and is already under construction, with completion scheduled for the second half of this year (Figure 3). Beyond that, initial plans are underway for further expansion of our manufacturing and cleanroom capacity on the near horizon.

Besides our production capacity expansion efforts, EVG has also significantly expanded its process development services. We launched our NILPhotronics® Competence Center and Heterogeneous Integration Competence Center™ (HICC) to serve as innovation incubators for our customers and partners, and shorten development cycles and time to market on new products and applications driven by advances in nanoimprint lithography, and system integration/packaging, respectively.

Our main goal with these centers of excellence is to provide flexibility and speed of process integration while ensuring the highest level of IP protection for every aspect of development. We work with customers and partners, ranging from start-ups to the world's largest manufacturers and research institutes to jointly develop processes with EVG at our headquarters in Austria as well as in our cleanrooms in North America and Asia. Our cleanrooms are outfitted with our most advanced

process tools and are designed to meet even the most stringent customer requirements, even allowing for virtual line concepts where wafers are reintroduced into customer fabs for further processing.

While adding new facilities and services is essential to EVG's growth, the most important ingredient to our success as a global semiconductor equipment company is our people. This year, we achieved a new milestone with our global headcount surpassing 1,300 employees from 29 countries. Since our people are our most valued asset, it is critical that we invest in the well-being of our employees. A case in point, family friendliness has always been a top priority at EVG, and this year marks the 10th anniversary of "EVG Minis", our in-house kindergarten and nursery, which provides free daycare to our employees. The EVG Minis started with eight children when we launched the program in 2013. Today, more than 60 children are looked after in two kindergartens and two toddler groups by a total of seven primary school teachers and five pedagogical assistants. We have already begun further extensions of the EVG Minis building as part of our ongoing construction projects.

EVG also firmly believes that it has a corporate responsibility to support a clean and sustainable environment. In recent years,



Figure 2: In November 2018, the Queen of 3D visited the site of EV Group's then-future Manufacturing III building at EV Group's corporate headquarters in St. Florian, Austria. From left to right: Clemens Schütte, Werner Thallner, Françoise von Trapp, Hermann Waltl, Paul Lindner, and Thomas Uhrmann.



Figure 3: Aerial view of EV Group's corporate headquarters in St. Florian, Austria. In the foreground are the completed Manufacturing IV and V buildings, as well as the Manufacturing VI building, which is under construction.



we have implemented numerous energy-saving measures as well as expanded green energy production on-site. Currently, we have more than 4,850 m<sup>2</sup> of roof area covered with photovoltaic panels, producing approximately 1.5 MW of power, with further expansions planned. Since 2020, the percentage of energy produced onsite with solar power versus our total energy production has increased by more than 4X. At the same time, the number of electric cars in our company fleet has increased by nearly 6X. In addition, our carbon efficiency ratio (the percentage of CO<sub>2</sub>-neutral and renewable energy versus total energy consumption) is nearly 75 percent. These are just some of the numerous green initiatives EVG is implementing to reduce its carbon footprint. We recognize the need to address climate change and we are committed to playing our part.

It is truly an exciting time for EVG. 3D and heterogeneous integration have brought fusion and hybrid bonding front and center as critical processes for continuing PPAC scaling. This has fueled tremendous growth within EVG, enabling us to continue to invest in our technology, infrastructure, and people, which in turn helps us to continue to invest in our customers' success. 2024 will be an amazing year for semiconductor innovation, with further advances in device architectures and packaging integration schemes such as backside power delivery, complementary FET, and 2D materials. Underpinning all these advances is wafer bonding, and as the market and technology leader in wafer bonding, EVG will be by our customers' side as they march forward on their roadmaps with smaller, faster, more power-efficient, and lower cost-of-ownership products.



## 40 Years of Industry Firsts at EV Group

EVG's strong investments in its products and solutions have led to many industry firsts over the years such as:

- The world's first double-side mask aligner with bottom-side microscopes, which enabled the widespread commercialization of MEMS products, in 1985
- The first production wafer bonding system for volume MEMS manufacturing in 1992
- Installation of the first production bonders for silicon-on-insulator (SOI) wafers in 1994
- Introduction of the patented SmartView® face-to-face wafer alignment technology in 1999, which revolutionized wafer-level packaging and 3D interconnects
- The industry's first integrated production wafer bonding system launched under the name GEMINI® in 2000
- The first temporary wafer bonding and debonding systems for ultra-thin wafers were introduced in 2001
- The GEMINI FB fusion bonding system, launched in 2009, enabled the production of the first backside illuminated CMOS image sensors as well as other 3D-IC stacked devices
- Launch of SmartNIL large-area nanoimprint lithography (NIL) technology, revolutionizing the high-volume production of optical devices, including AR waveguides and optical sensors, as well as medical and bioMEMS devices in 2014
- BONDSCALE™, our next-generation fusion wafer bonder for "More Moore" scaling and front-end processing to address future logic transistor scaling and 3D integration challenges outlined in the IRDS Roadmap, introduced in December 2018
- The LITHOSCALE® maskless exposure lithography system unveiled in September 2020, which brings the benefits of digital lithography in high-volume manufacturing to a wide range of applications and markets, including advanced packaging
- EVG®850 NanoCleave™ layer release system, introduced in 2023, enables nanometer-precision release of bonded, deposited, and grown layers from silicon carriers using an IR laser – thereby eliminating glass substrates for advanced packaging and enabling thin-layer 3D stacking

# The Year in Test

By Mark Berry, COT-NPI Group LLC

Is test non-value added? Certainly, some aspects are unchanging. Test is one of the three means to guarantee parts in addition to characterization and the design itself. Given the market backdrop – across automotive, computing, and advanced packaging – new test challenges and value adds have emerged.

challenges especially when using logic from various process nodes. One example is new physical stress mechanisms and a higher probability of interconnect failures.

The IEEE 1838 specification for die-to-die stacks is another example of a "shift left" in bringing design and

"Shift Left" More Concurrent Test Development
<ul style="list-style-type: none"><li>• 2025 ASIC design releases &gt; 16,500</li><li>• Time to adoption (100M users) – cell phones 16 years – ChatGPT 2 months</li><li>• LS ADAS – self driving – 1B lines of code</li><li>• Micro bumps becoming impossible to probe</li></ul>

Unify the Flow – End to End Sharing, Faster Action across Test Flow
<ul style="list-style-type: none"><li>• Automotive reliability levels in PPM – MCU &lt; 0.5, ASIC &lt; 0.2, flash &lt; 0.1</li><li>• Automotive zonal approach raises CPU / car from 12 to 48</li><li>• 3D logic stacking challenges</li><li>• Flash scaling has reached zeta bytes</li></ul>

Combating Silent Data Corruption (SDC) Within a Test Budget
<ul style="list-style-type: none"><li>• Infant mortality – advanced process node and packaging – on the rise</li><li>• Transistors slowing with age</li><li>• 10M servers in use across big 5 firms with 3-6 year service life</li></ul>

Three main themes are "shift left", which is the need for more concurrent development with ever-increasing dependencies between design, packaging, test, and field operation; greater unification in development, production, and across the end-to-end test flow; and the continued war on silent data corruption (SDC) – balanced with test economics (Figure 1).

## What is Shift Left?

The term "Shift Left" has been used increasingly within development to indicate tasks that were once performed sequentially but must now be done concurrently. This is usually due to tightening dependencies between tasks. Several types of "design for..." approaches are taking hold as tools within a broader design for test (DFT) umbrella: S (stress), R (reliability), I (inspection), and O (observability). Beyond test, some automotive firms are using S (security) and S (safety).

In simpler products wafer probe was an acceptable means for determining Known Good Die (KGD) as a gross screen before assembly. Now there is far too much value in an 8 FET SiC module [1] or 2.5/3D compute multichip modules such as system-in-package (SiP) and chiplets. The probe must produce as close to KGD as possible. With many forms of advanced packaging, all the interconnects must be checked regardless of accessibility – hence the term known good stack (KGS) and overall known good system (KGS).

The Universal Chiplet Interconnect Express (UCIE) specification [2], aimed at die-to-die, has been upgraded to 1.1 addressing more protocols and broader usage models. As 3D die stacking evolves from high-bandwidth memory (HBM) memory to logic, there are new

test closer. KGx starts with the architecture and product planning, needs to be supported by the design, and is delivered by test and assembly operations.

More complex test flows and more expensive bill-of-material (BoMs) require greater unification across the end-to-end test flow for development and action in production.

Automated test equipment (ATE) and system-level test (SLT) linkage shows a huge increase in the need for SLT after ATE test. SLT can be as much as 50-100x less expensive than ATE, but it historically has been an "island" running very different and long (think 20 minutes) algorithms reflective of end customer use cases.

Intel notes that many of its customers run SLT for much longer periods than the company does. Many advances by Teradyne and Advantest facilitate more feed-forward and feedback of test patterns from the two environments to make initial test development results in improved reaction times to enhance upstream ATE test when new failure modes appear at SLT. Other examples include doing more analytics on the tester on the fly. The benefits of this include adaptive tests. For example, if a given batch of material (wafers, finished goods) is exhibiting certain parametric around process corners (fast/slow transistors, high/low power) then the test program can be adaptively and dynamically varied. ATE makers have placed more of these tools within the tester for real-time decision-making, as opposed to a central test floor computer.

Continued on page 71

# Thermal Simulation of a Packaged GaN MMIC

By Casey Krawiec and Erik Sanchez, StratEdge Corporation

StratEdge has been designing and manufacturing packages for high-power, high-frequency compound semiconductors since the early 1990s, with much attention focused on gallium arsenide (GaAs) and gallium nitride (GaN). Because of its ability to operate at very high currents and high voltages, gallium nitride GaN is widely used in applications for high-power devices operating at high frequencies. While much attention is given to GaN devices, what is often overlooked is the package in which the GaN device is attached and the way the device is attached to the package. It's well known that GaN device efficiency and reliability can be improved by creating a package environment that reduces chip-to-package junction temperatures (TJ).

GaN devices, especially GaN on silicon carbide (SiC) devices, can handle higher temperatures allowing designers to make circuits smaller. The GaN chip can produce much greater power density, but it becomes the package's job to help remove the heat that is generated. The goal is to increase the power output that a device can achieve, thereby maximizing its performance. Therefore, it is important to provide the most efficient way to dissipate the heat so the device isn't as likely to overheat and fail from normal operation.

The challenge is finding a suitable package for GaN because of its extremely high power density. What makes the package more suitable is a heat-spreading base made with a high thermally conductive material. The epoxy or solder material used to mount the GaN device onto the base is also important since the heat generated by the device must pass through this layer.

The thermal conductivity of the base material is not the only consideration. Its coefficient of thermal expansion (CTE) is also critical. The high temperatures produced by GaN require a base with high thermal conductivity and a CTE matched to the GaN device. Engineered materials like copper tungsten (CuW) composite and laminated copper-molybdenum-copper (CMC) were developed within the industry to construct robust packages.

While copper is an excellent heat conductor with a thermal conductivity of about 400 W/mK, it expands greatly when it becomes hot compared to the GaN device. Bases made with CuW composites combine the desirable thermal conductivity of the copper with the stiffness provided by the tungsten, but experimentation found that bases made with laminated

balance of thermal dissipation and expansion match for the base material. The effective thermal conductivity in the z-direction is close to that of CuW, which is about 190 W/mK. What CMC provides that CuW does not is a layer of copper directly beneath the GaN device. This enables the heat to spread away from the hot spots on the bottom of the device, which helps reduce the TJ.

StratEdge recently conducted a series of thermal simulations to compare how well heat is dissipated from a GaN device. This article explains the boundary conditions of the simulations and presents the results using various die attach and base materials. For this study, materials were used that have CTEs known to match that of GaN-on-SiC; therefore, the effects of potential mismatches are not discussed. So

Copper-molybdenum-copper (CMC) Base Composition, Layer Thickness (inches)	Copper tungsten (CuW) Base Composition, Layer Thickness (inches)
Copper (401 W/mK), 0.002	Copper tungsten (190 W/mK), 0.010
Molybdenum (139 W/mK), 0.006	
Copper (401 W/mK), 0.002	

Figure 1. Base materials and thicknesses studied.

layers of copper and molybdenum proved to be the best fit for GaN. Molybdenum, while not a great thermal conductor, is stiff and can be laminated to copper to provide a core that enables the entire base to have a good CTE match with the GaN device. CMC, constructed with a 1:3:1 ratio, results in an optimum

too for the die-attach materials. The modulus of elasticity of solder alloy versus organic polymers can be important as are many other factors, but the focus of this study is on heat transfer and the TJ of the device. The TJ is the highest operating temperature of the bottom of the GaN device in the package. As

Die Attach Materials	EPO-TEK® H20E Silver-filled Epoxy	Gold-tin (AuSn) Alloy Solder
Bond Line thickness (inches)	0.0015	0.00025
Thermal Conductivity (W/mK)	2.5	57.0

Figure 2. Die-attach materials and bond line thicknesses.

mentioned above, the TJ has a direct correlation to reliability; the lower the TJ, the longer the device lasts.

We will compare two different base materials, CuW (15% Cu/85% W), and CMC, to determine the effect they have on TJ, all other things being equal (Figure 1).

We then compare gold-tin (AuSn) solder alloy to a traditional silver-filled epoxy (H20E) (Figure 2). There are different methods for AuSn die attach. StratEdge chose scrubbing, which is the process of heating with mechanical agitation. It's the extremely thin bond line, which can only be achieved with the scrubbing process, that optimizes heat transfer and results in a near void-free attachment. In addition to providing superior thermal performance, AuSn solder can be used for high-reliability applications because it won't outgas, and it is unlikely to fail if done properly.

## GaN MMIC and Package Simulation Model

The device used in the model is a 10-watt high-power GaN MMIC with three output stages. It is 0.1498" in length from RF-in to RF-out and 0.1134" wide. The output stages are evenly spaced 0.0375" from the output end of the device and each generates 3.333 watts. The device is attached to a metal heat spreader that is the base of a ceramic package. Both the package and heat spreader are 0.450" square in size. The metal base is 0.010" thick. The device is 0.004" thick.

To perform the steady-state thermal analysis, a model was created that mirrored the packaged device assembly (Figure 3). As in the actual assembly, the device is offset from the center of the package. The package used was an off-the-shelf StratEdge Leaded Laminate (LL) Series package, part number LL4545-0-2, with broadband RF performance from DC to 63 GHz. The device's RF output port was aligned next to an RF pad on the package as close as possible to the cavity wall so that the ribbon connecting the device to the package was as short as possible. StratEdge packages are manufactured with essentially no

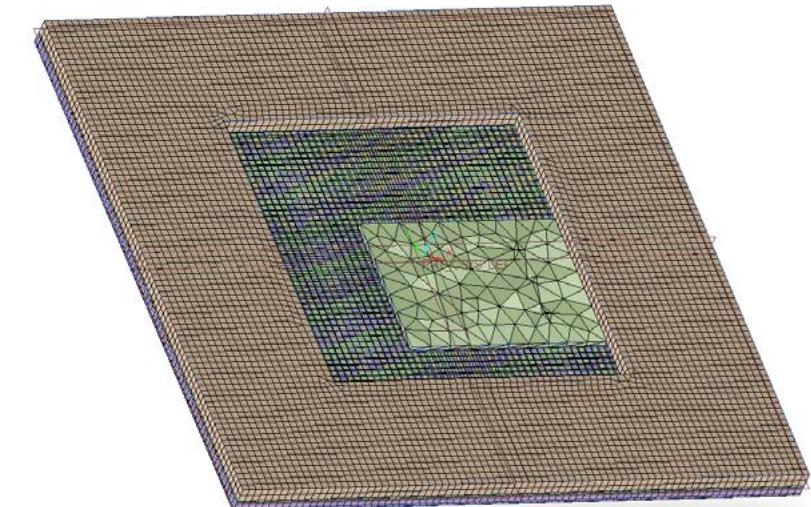


Figure 3. 3D simulation model.

braze fillet, which allows the device to be mounted practically touching the ceramic cavity wall at the output side of the package.

The simulation software used was PTC CREO developed for use with Ansys. The boundary conditions for the model were a 0.00025" wide border within the perimeter set at a constant 75°C. The 10 watts generated by the device were divided equally over the three output stages. Each stage was 0.00039" wide by 0.00087" long. The software program allowed each stage to be divided into eight 0.00015" square elements with 0.00009" spacing between them.

## Comparisons of CuW to CMC and Silver-Filled Conductive Epoxy to AuSn Solder

Using the above model, the peak output stage temperature of the device attached using H20E on a base made from CuW (15% copper) was compared to the same mounted on a CMC base. Refer to Figure 2 for all bond line thicknesses. The TJ for the model with the CMC base was 272.9°C, which was 8.9°C cooler than the model with the CuW base. Then the model with the CuW base and H20E die attach material was compared to the same base with AuSn solder die attach material. The TJ for the model with AuSn was 257.3°C, which was 24.5°C cooler than the model with the H20E. When the model for die attached to CuW with H20E was compared to CMC

attached with AuSn, the TJ dropped to 247.3°C, which was 34.5°C cooler. The simulation indicates that the device mounted onto a CMC base using AuSn with a bond layer of about 0.00025" runs at a significantly cooler temperature than the device mounted on an industry-standard base material with die-attach epoxy.

The results were consistent with those reported by an independent party who made thermal measurements of a similar high-power GaN amplifier assembled under the same two configurations.

## Summary and Conclusions

To quantify the benefit of mounting GaN devices with AuSn solder with ultra-thin bond lines into a package with a CMC base, a model was created for a 10-watt high-power GaN MMIC. The simulation showed that attaching this device to CuW using H20E created a TJ that was 34.5°C hotter at the hottest junction for the same device mounted on CMC with AuSn. Measured verification of the study results is in process but not yet available. Using StratEdge's proprietary eutectic die attach method to attach a GaN chip to a StratEdge LL Series package made an amazing difference. By using packages with CMC bases and the AuSn eutectic die attach method that uses mechanical agitation and heat, chip temperatures are reduced, which improves the efficiency and reliability of the device.

# Balancing Precision and Throughput in 3D Structures with Advanced Packaging and Motion Control

By David Doyle, HEIDENHAIN

The relentless drive in the semiconductor industry to consistently deliver improved performance and power efficiency has traditionally led to increasingly smaller device geometries. However, these tiny footprint dimensions are starting to hit upon a process complexity and are becoming overly expensive to manufacture. Nobody can deny that keeping up with Moore's Law has always been a challenge, but perhaps it may be time for a sober discussion.

The alternative approach presented herein implies a general transition to advanced packaging methods and 3D structures, where the objective of continuing to improve the speed, scale of compute capability, and power efficiency of new semiconductor products supporting AI applications can be achieved without only shrinking the basic geometry of the semiconductor device.

In fact, advanced packaging methods offer new integration strategies that combine technologies at the modular level, through chip-to-chip interconnect technology that enables the combination of high-yielded small-die processes, into larger and more complex integrated multi-chip systems, without advanced node gate level technology for large single-die dimensions that are more challenging to yield. But, while the individual device geometry may relax, these new approaches are, nevertheless, placing heavy demands on ever-greater precision and alignment to realize the integrated system design and the necessary production process control.

This, of course, requires motion control technologies to keep pace with these requirements for unprecedented, combined speed, accuracy, and precision (Figure 1). Concurrently, nobody wants to see throughput metrics decrease, which creates a constant drive for increased accuracy and precision at high production throughput.



Figure 1: HEIDENHAIN linear encoders are accurate, compact, and reliable.

## Demands for Increased Precision

An example of one such relatively new manufacturing process is die-to-wafer hybrid bonding, where dies are stacked one on top of each other and interconnected via fine copper interconnects. This enables a previously unachievable density of connections, surpassing the limits of conventional copper bump technologies and considerably minimizing signal delay and attenuation.

However, a higher density leads to tighter tolerances, and thus far more accurate motion control in the bonding process is needed than is the case with conventional alternatives.

Another new development in this segment is fan-out wafer-level packaging (FOWLP) including new more stable substrates. Despite having been invented more than 20 years ago, fan-out package design has garnered substantial interest from today's market and is currently seen as a worthy alternative to fan-in, particularly over the last five to ten years.

Compared to standard wafer-level packages, FOWLP enables impressive input/output specs within a more compact footprint, while also delivering superior thermal and electrical performance. As the die gradually becomes smaller, fan-out packaging enables the very high interconnect densities that are present on smaller dies.

Unfortunately, the required production process is quite complex. FOWLP requires the reconstitution of the wafer with a die embedded into low-cost materials, which enables high-cost silicon to become more efficient. However, this process is coupled with precise fabrication steps, which slow down production, challenging producers' cost-of-ownership (CoO). The relationship is clear: the higher the density, the finer the connection pitch, and the higher the placement speed and accuracy requirements.

## Balancing Accuracy and Throughput

Tool selection in the semiconductor industry is predominantly driven by CoO. For back-end applications, CoO is typically defined as a combination of cost per bond and yield. Both metrics are directly linked to positioning accuracy and throughput of the motion system used in the chip integration process (Figure 2). There is no tolerance for yield loss of finished ICs, therefore the reliability of the packaging integration process needs to be extremely high.



Figure 2: ETEL's TELICA motion system for precision backend semiconductor processes

One can have all the bandwidth, AI, and optics in the world, but none of this really matters when a semiconductor tool cannot achieve nanometer-level precision

without compromising production throughput. When the goal is to take high-precision measurements as quickly as possible, the maximum speed of a motion system's axis must be delivered with minimum settling time or measurement on the fly. There are usually multiple tradeoffs present and thus, by design, conventional motion system architectures are optimized either for high positioning accuracy or for high throughput.

To achieve the coveted combination of speed, accuracy, and stability, more advanced processes and motion technologies are needed, i.e., encoders for capturing position and speed, as well as motion control systems for high-precision movement of tools and components.

## Motion Systems Set to Assume a Leading Role

Advances such as FOWLP introduce multiple variables into the production process, creating a higher probability

of imperfections in the final product. Furthermore, this approach also requires extreme speed and consistent pinpoint accuracy for efficient, profitable semiconductor manufacturing.

There are two core technologies that are proving decisive in achieving success with this new production strategy. The first key element of this approach is the very compact HEIDENHAIN LIP 6000 encoder that delivers an impressive signal stability of 0.4 nanometers at 1 MHz, enabling the motion system to achieve millisecond-level seek and settle times. Secondly, ETEL controls utilize algorithms to calculate the optimal path performance for inspection similar to those that are used to help race car drivers follow the most optimum racing line.

ETEL's TELICA motion system is an advanced high dynamic motion system platform dedicated to precision backend semiconductor processes that enables the process

to achieve sub-micron placement accuracy required for advanced, next-generation packages. This high level of accuracy is maintained over a work area of up to (870 x 800 mm), which concurrently enables very high-duty cycles and throughput.

TELICA is now introducing an entirely new approach comprising a secondary metrology loop at the process plane level. This drastically reduces Abbé errors as well as the relative positioning mismatch between the process tool and substrate. Multi-dimensional encoders ensure that the placement accuracy level is achieved in up to six degrees of freedom, while water-cooled 'iron core' motors enable extreme yet reliable duty cycles.

Continued on page 71



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# When Plasma Matters: Three Reasons to Choose Plasma

By Peter Dijkstra, Trymax Semiconductor

Every metal layer on a wafer, from M1 at the front end to redistribution for wafer-level packaging (WLP), requires patterning. Selective material removal, including etching oxides and metals, often becomes the critical path. It is essential to thoroughly strip photoresist and minimize contamination to achieve the desired yield. Plasma etching enables successful results.

The finer the features and the greater the number of layers, the more necessary it is to achieve precise, repeatable patterns during lithography. Vertical architectures like 3D NAND with many layers and high aspect ratios (HAR) step up the processing challenge. The structures need vertical sidewalls and contamination-free surfaces. The process window is extremely narrow. Every deposition and etching step must be optimized, or yield will suffer.

Two general approaches for removing material from a wafer surface are wet chemical etchants and dry plasma etching. Choices between the two technologies depend on multiple factors, and fabs will often use wet and dry processing

together, selecting the best option for each process step or product type. There are often tradeoffs between speed and selectivity that need to be considered to achieve the best result.

Plasma etching is used in several different process steps. These include:

- Etching of oxide, nitride, metal, and polyimide layers
- Ashing to strip the photoresist after patterning metal and oxide layers
- Descumming to remove any photoresist remaining after patterning each layer

This article discusses plasma etching technology, focusing on reasons to choose plasma over wet etching. It comes down to three things: process flexibility, consistency, and traceability.

## Tailoring plasma etching

Plasma etching is precise, flexible, and compatible with many different processes. Depending on the gas used to create the plasma, it can

remove metals or dielectrics from various substrate materials.

Adjusting the gas composition, pressure, flow rate, and temperature affects the etch rate and selectivity. Precise tailoring of the plasma chemistry allows plasma etching to be highly selective, removing the target material while leaving other areas of the wafer untouched. In practice, it can take extensive modeling and testing to develop a recipe that will achieve the necessary selectivity and not damage previously deposited layers.

Plasma can be made from a wide range of gasses, including oxygen, hydrogen, nitrogen, helium, methane, and more. Ashing, for example, uses oxygen plasma at a temperature of around 250 °C to burn off the photoresist. The descum process is much gentler and runs at a lower temperature.

The power source generating the electricity needed to ionize the gas to form plasma can be radio frequency (RF), microwave, or a combination of the two. Multiple reactor types (Figure 1) allow for greater flexibility in processing conditions. Facilities

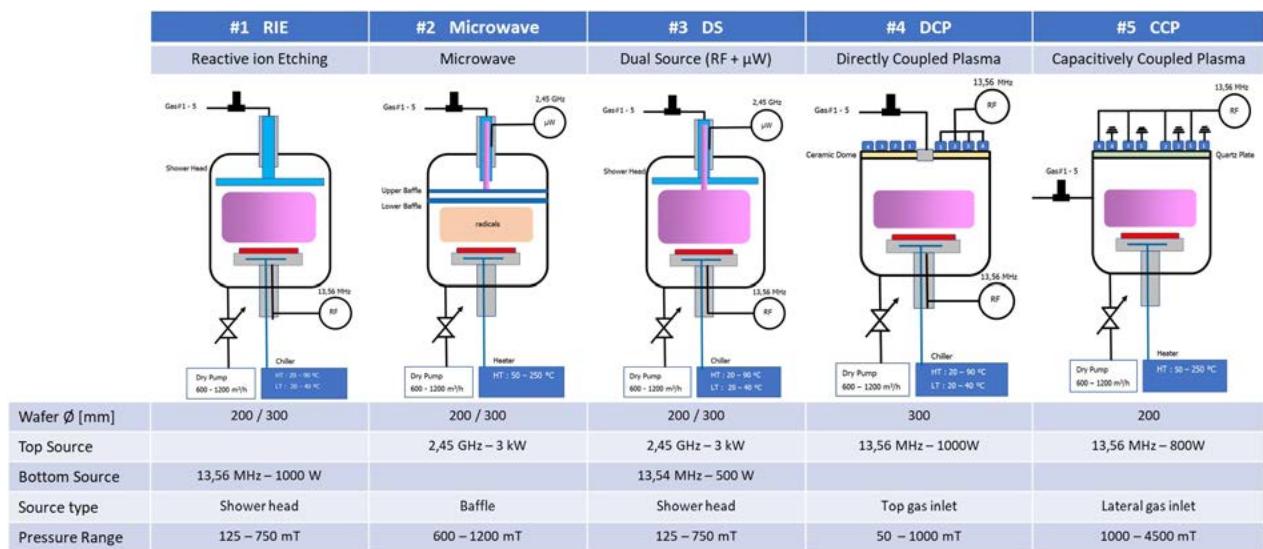


Figure 1: Schematic showing types of reactors for plasma etching.

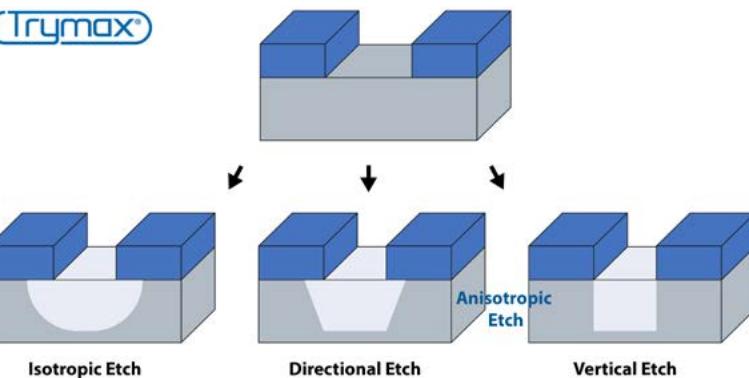


Figure 2: Isotropic and anisotropic etching options available with plasma etching.

can select the option that best meets their temperature and pressure requirements, and choose equipment that fits into their process flow and available footprint.

Other options include capacitively coupled or inductively coupled plasma. Capacitively coupled plasma has typically been used for etching dielectrics, while high-power inductively coupled plasma is more commonly used for etching metals (Figure 1).

Plasma offers excellent etch control, including controlling whether material removal is isotropic (the same in every direction) or anisotropic (faster removal on one part of the surface), as shown in Figure 2. This flexibility is especially beneficial for removing layers from trenches in HAR structures. Controlled anisotropic etching minimizes the risk of over-etching the bottom of the trench to achieve sufficient material removal from the sides.

## Consistent Results

Consistent results from wafer to wafer are necessary to maintain high, repeatable yield. Consistency is another aspect where wet and dry etch differ.

Wet etch immerses an entire cassette of wafers at once. Each batch that goes through the process affects the bath chemistry. The first wafers that go through after a bath change will experience pristine, ideal conditions. By the time later batches go through, contamination or chemical degradation can cause the yield to drop. More frequent bath changes can mitigate this effect, but that increases chemical consumption and waste.

Plasma chambers usually process one wafer at a time under conditions that remain stable. Once input parameters are set, the gas flow rate and pressure are always the same. Continual monitoring will flag any deviations and pause processing.

The substrate temperature is also monitored and controlled. Because plasma process conditions can be tailored to the materials and requirements for each application, and wafers are processed one at a time, consistency is easier to achieve (Figure 3).



Figure 3: High-speed wafer transfer via the Trymax equipment front-end module.

## Better Traceability

One-by-one processing also improves process control and traceability. The process will stop if data shows that a measurement is out of specification. A technician will make the necessary adjustments and restart the equipment. At most, one wafer will be affected versus an entire cassette.

If inspection further down the line shows repeating defects, data on every wafer that went through the plasma chamber is available. Analyzing this data can indicate whether anything in the plasma process was responsible for the yield loss, improving traceability and failure analysis. This option is not available with batch processing.

Automotive and biomedical markets are especially sensitive to the need for repeatably producing reliable devices, as human safety is in play. They want to see comprehensive failure analysis and appreciate track and trace capabilities at the wafer and chip level.

## Conclusion: The Need for Plasma is Growing

While wet etch is not going away, and some products and process steps are well-suited to wet etch, we believe that plasma use will continue to accelerate. At advanced nodes, some geometries cannot be patterned with wet etch. Power integrated circuits (ICs) for automotive and 5G applications are often built on silicon carbide (SiC) or gallium nitride (GaN) substrates for greater efficiency in high-voltage, high-frequency operating environments. Standard wet etchants do not work on these materials. This is a growing market where the flexibility of plasma etch can meet the requirements.

Another reason the plasma market is growing is the increasing demand for tracking and tracing at the wafer and chip level. This requirement will expand beyond the automotive and medical industries to more applications.



Figure 4: Easily accessible process modules allow for customized solutions.

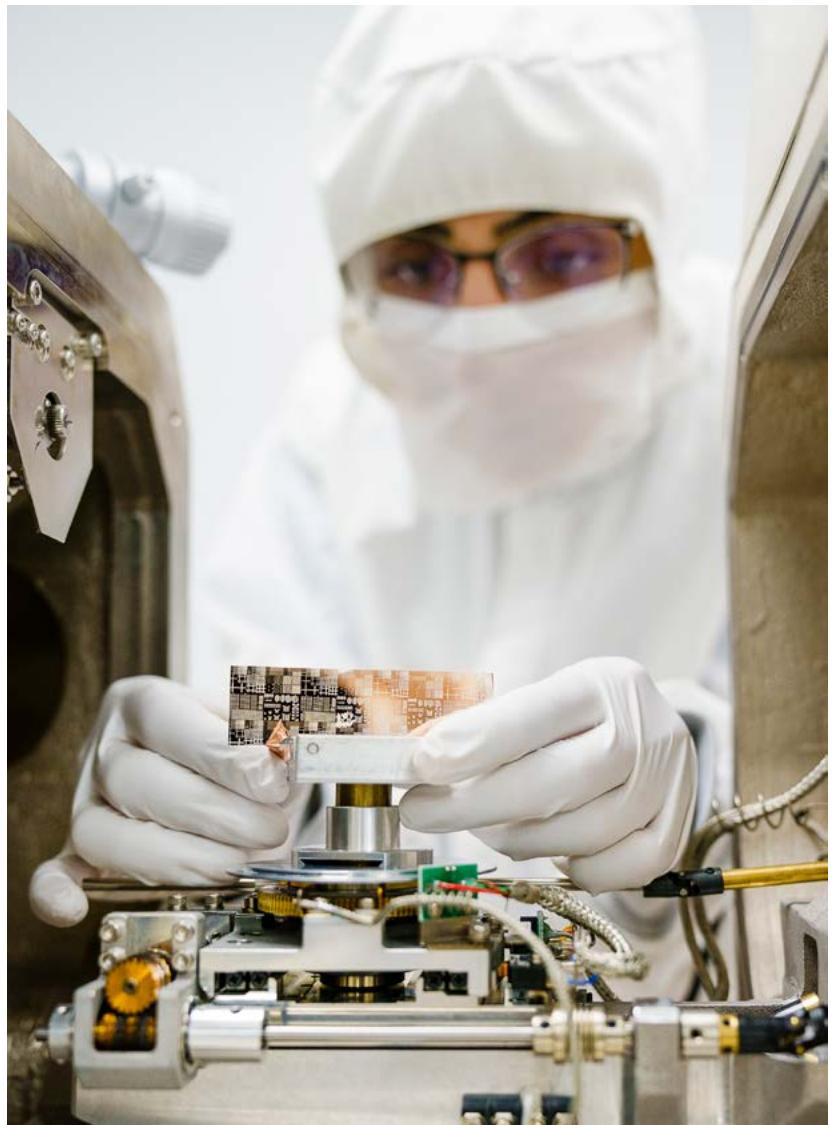
There is a need for machines that can take full advantage of the flexibility of plasma processing (figure 4). Tools like the Trymax NEO series that can handle a wide range of input gases, switch between sources, handle different substrates, and process multiple wafer sizes are well-positioned to serve the entire semiconductor industry.

# Bridging the Path from University to Industry

By Rene Dubois, ClassOne Technology

The university setting offers a valuable environment for future engineers to explore and learn about technologies that will become part of their daily lives when transitioning from school to a career. At the same time, universities working on microelectronics and advanced R&D are increasingly looking for more advanced manufacturing equipment that offers both reasonable upfront investment cost, and a low cost of ownership.

Over the next five years, we will see significant changes in the kinds of microelectronics projects and programs universities pursue. University fabs are moving toward



advanced fab-level wafer processing and away from the benchtop beakers and wet benches that were not equipped to deal with new and emerging challenges. With the passage of the U.S. CHIPS and Science Act, universities are looking to take a major leap forward in the capability to transfer technology more readily to the chip manufacturing industry.

Engaging with advanced tools is also more interesting than working with wet benches, which will inspire students to join the industry and be better prepared to work in real fabs. This will be vital to filling the semiconductor industry's need

for skilled workers. According to a recent **Semiconductor Industry Association (SIA)** report, the workforce will grow to approximately 460,000 jobs by 2030, representing 33% growth from today's 345,000 jobs. However, at the current degree completion rate, 58% of these projected new jobs (and 80% of projected new technical jobs) may go unfilled.

Universities are thus under added pressure to attract and excite students to enter the industry by providing relevant curriculums and imparting real-world skills. Bringing more advanced tools to universities will also mirror what's being used in the semiconductor industry – essentially setting up universities to become an adjunct for industry development.

Some university cleanrooms are already adding the kinds of production-proven, fully automated high-volume tools found in today's semiconductor facilities. While this level of investment is aspirational, other schools plan to spend significant funds on their cleanroom setups. They need affordable yet powerful tools to help them move toward industry-level offerings that allow them to optimize premium fab space.

## Enabling the Lab-to-Fab Transition

Many universities looking to offer more leading-edge capabilities focus on advanced packaging (AP). According to market research firm Yole Group, this industry's market value is projected to grow from US\$ 44.3 billion in 2022 to US\$ 78 billion by 2028 – a 10% CAGR. AI and machine learning enable data centers, automotive, 5G, and other applications that require powerful processors to handle the sheer volume of generated data. In turn, these devices necessitate the use of AP techniques.

Continued on page 72

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# Semiconductor Industry Marketing and Communications: Learning by Doing

In this 2024 issue of the 3D InCites Yearbook, we continue our tradition of featuring essays written by interns in the field. This year, we have contributions from two recent graduates who are exploring careers in semiconductor marketing and communications.

## Navigating the World of Semiconductors: My Journey at Megatech

By **Erwan Amade**

The semiconductor industry lies at the heart of almost every technological innovation of our time. For those looking to delve into this fascinating world, my experience might serve as a guide.

### My Education: Balancing Science and Commerce

My journey began at the IUT Chemical and Process Engineering in Lyon, where I gained a strong foundation in chemical engineering. This base opened the door to the semiconductor universe through an internship at CEA Leti for Entegris. Wishing to blend technology with business, I continued my studies at HYBRIA, merging technical expertise with commercial strategy.

### My Adventure at Megatech

Megatech is a UK company with 30 employees, celebrating 50 years as a recognized distributor in the



semiconductor sector. When I started this placement, I knew I was about to embark on a rewarding adventure. What I hadn't anticipated was the depth and diversity of experience that awaited me.

One of the most significant tasks entrusted to me was the entire management of our presence at the **European Microelectronics and Packaging Conference 2023** in Cambridge. This was a new event for Megatech. Beyond mere logistics, my role provided a deep dive into the semiconductor industry.

The scientific aspect of this endeavor mainly revolved around product selection, leading me to deepen my knowledge through training sessions guided by experts in the field. This immersion granted me an insightful perspective on the intricacies and vastness of the semiconductor sector.

On the commercial side, I developed a digital marketing and communication strategy.

Merging my newfound technical knowledge with market needs, I crafted impactful campaigns to highlight our presence at the event.

The exhibition itself was a whirlwind of activities. Representing Megatech, attending various conferences on the latest innovations, interacting with diverse exhibitors, and capturing leads were central to my duties. Each conversation and every handshake brought

me closer to a comprehensive understanding of the industry.

Following the bustle of the exhibition, I delved into the digital realm, revitalizing Megatech's presence on LinkedIn and YouTube. Analysis, planning, and content creation became my daily companions. I discovered the power of digital storytelling and the significance of a professional platform like LinkedIn for a company's growth.

Beyond tasks and projects, it was Megatech's culture that resonated most with me. The sense that my work mattered, that my voice played a role in decision-making, allowed for my professional flourishing. Product training sessions, daily interactions with industry professionals, and the freedom to explore deepened my passion for the semiconductor realm.

### Final Thoughts

Looking back, I recognize the transformative nature of this experience. Not only did it equip me with skills and technical knowledge, but it also ignited my inspiration to continue down this path. To anyone aspiring to progress in the world of semiconductors, I would say this: dive in without hesitation. It's a constantly evolving sector, with each day ushering in a wave of innovations and challenges. Immersing oneself in this field means being at the heart of technological advancements shaping our future.

## Learning About Strategic Semiconductor Communication: My Internship at Kiterocket

By **Mindy Lok, Kiterocket**

I am passionate about the emerging and leading technology shaping the world. After accepting an internship at Kiterocket, a global PR and marketing agency, I quickly delved into learning about the technical and complex world of semiconductors. This internship allowed me to grow the skills necessary to excel in an agency that supports clients focused on creating innovative technology.

It was exciting to research the key players and competitors in this industry and learn about the advanced terminology and jargon often used in various forms of strategic communication. I also watched in-depth training videos on the important facets and processes that many of the agency's clients are responsible for in the industry.

I was mentored by some of the brightest veterans and peers in public relations, digital marketing, technical writing, brand strategy, and account management. Working with team members in a collaborative and creative work environment inspired me to become a more well-rounded communications specialist.

Throughout my internship, I became more confident in my ability to produce valuable deliverables such as media lists, event lists, quarterly reports, media briefing books, weekly meeting agendas and recaps, social media posts and graphics, email newsletters, blog posts, and more.

During my first week as an intern, I wrote a blog post for a client focused on encouraging people to join their company. I enjoyed the experience as I had never written a blog for a client before and was able to write creatively on an unfamiliar topic. Additionally, creating social media posts and graphics for different clients was also a great learning experience as I was able to craft posts that aligned with the unique brand image and messaging of different companies.

Another memorable project I worked on was creating a trade show opportunities list from scratch for a client that helps innovative startup companies grow their businesses. To do this, I researched trade shows and conferences taking place



throughout the year that the client could attend or exhibit to boost the company's brand awareness.

Overall, my internship was a rewarding, positive, and welcoming learning experience. I enhanced my capabilities in public relations and digital marketing with B2B clients and better understand how to best support clients in an impactful way. Kiterocket has a knowledgeable team that is open to making the internship experience as fulfilling as possible for aspiring strategic communicators.

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## 3D InCites Community Member Reflections: How Are We Addressing the Global Talent Shortage?

After a downturn in 2023, the semiconductor and microelectronics industries are expected to rebound in 2024 and beyond. As the US and EU Chips Act Funding begins to be dispersed, one of the ongoing challenges is finding the workforce needed to help these industries grow.

For this year's community reflection, we asked our members how their company is approaching the global talent shortage. What challenges are they facing in their regions of the world, and what are they doing to address them? Here, four member companies share their stories: Trymax Semiconductor, Onto Innovation, ERS electronic GmbH, and Mosaic Microsystems.

### How Trymax is Navigating the Talent Shortage

*By Tessa Baltussen, Trymax Semiconductor*

The “Global Talent Shortage” is a buzzword that everybody uses nowadays. But what does it mean? The most used definition I found was that *employers cannot find the people they need with the right blend of technical skills and human strengths*.

The talent shortage is a significant concern in the U.S. economy, with the overall talent deficit expected to reach 600,000 by 2030 in the financial and business services sectors alone. This issue is closely followed by China, Japan, Germany, and the U.K.

The Semiconductor Industry Association (SIA) released a study on July 25, 2023, that highlighted a pressing issue: the U.S. is currently grappling with a substantial shortage of technicians, computer scientists, and engineers. According to the study, there is a projected



shortfall of 67,000 workers with these skill sets in the semiconductor industry. This talent scarcity is not limited to the U.S. alone, as evidenced by ASML's quest to hire an additional 4,000 engineers. Clearly, this issue is not confined to one region but can indeed be classified as a global shortage.

The impact of the talent shortage can have far-reaching consequences. It can lead to a series of challenges, including increased costs, decreased productivity, and missed opportunities for growth. It can also create social unrest as people who can't find good jobs become frustrated and angry. Fortunately, there are strategies businesses can use to overcome the talent shortage.

#### Look beyond the resume and the available position

At Trymax, we look for hidden talents, growth potential, and the broader contributions an applicant can make to the organization, rather than just matching their qualifications to the job description at hand.

#### Nurture existing talent within the company

We invest in the growth and development of our employees to help them reach their full potential while contributing to the company's long-term success. It's a proactive approach to talent management that benefits both the individual employees and the organization as a whole.

#### Take a data-driven approach to recruiting, e.g. sourcing analysis

Data-driven methods can enhance recruitment by improving decision-making, efficiency, and candidate experience while reducing costs and biases.

#### Involve employees in the process of finding new team members

This can be achieved through initiatives like an employee referral program, and also by including employees in the interview process. Their insights are invaluable for describing the job responsibilities and providing a glimpse into the work culture at Trymax.

Once hired, the next concern is how to keep talent. It is widely acknowledged that top-notch professionals are more likely to leave an organization if they find the company's processes disengaging. Top-notch professionals are driven by a combination of challenging work, opportunities for growth, recognition, and a positive work environment. This is precisely the ethos we uphold at Trymax. We ensure that talent feels responsible, well-accepted, and respected in their team and the organization. In other words, every person is seen and recognized.

## Fostering Innovation from Within

*By Tom Bauer, Onto Innovation*

As many organizations in the industry are grappling for external resources, Onto Innovation has expertly chosen to look inward. We recognize the unmatched talent that exists at our company already and have implemented a course of action that directly taps into that. Our employees continuously push the boundaries of innovation, so their long-standing commitment to Onto is nothing but an asset.

Onto talent has grown 40% since 2022, but despite the infusion of new talent, our average employee tenure is almost eight years. This centralized focus on employee retention has thus become the core of our strategy moving into 2024.

We have found that encouraging, educating, and advancing our workforce are key in this initiative to keep our employees satisfied in their professional careers. To achieve this, our human resources team has aimed to increase current employee ascension throughout the organization. Providing vertical and lateral movement opportunities ensures that our current talent is being used to their fullest potential and that their history with Onto is rewarded.

In 2022, this growth initiative provided approximately 20% of our team with promotional opportunities, well exceeding the 7% average documented by the Society for Human Resource Management Human Capital Benchmarking Report.<sup>1</sup> Thus, our engineers

and other employees are exposed to a broader set of opportunities. They get to expand their skills by learning alongside other groups, ultimately leading to improved industry problem-solving and technological innovation. Concurrently, our employees' drive for excellence is reignited as they tackle these new job tasks, generating higher employee satisfaction.

This retention plan works hand in hand with our strategy to invite newcomers to Onto. Our employees join and stay because of our attentiveness to their needs. We have established structured engagement programs to ensure that our employees feel supported. Our Buddy Program helps new hires integrate into life at Onto through the guidance of a current employee. We host learning opportunities covering topics on emotional intelligence, active listening, leadership competencies, and more. We prioritize the benefits of in-person interaction in a meeting room, in the lunchroom, or on the clean room floor. And Onto understands the needed balance of disconnecting outside of work hours.

Now more than ever, it is imperative that our human resources team is intentionally aligned with our business model to make effective talent-based decisions. We make it a priority for the team to understand the deep programmatic needs of the company and the technicality of our industry. They leverage analytics around lead time and critical high-volume needs to ensure proper timing and pipeline health for critical path resources.



We also partner with organizations like The Society of Women Engineers and Hack Diversity to broaden our reach and advance diversity of team thought. Our core contingent global staffing partners are also available to support the ebbs and flows of the business as we navigate the current climate.

## Fueling the Workforce Through Investment and Engagement

By Sophia Oldeide, ERS electronic GmbH

It is an exciting time to be an equipment manufacturer in the European semiconductor industry. There is still a lot of buzz around the EU Chips Act and companies like Intel, TSMC, and GlobalFoundries & STMicroelectronics have announced huge investments in Europe over the next few years. However, Europe is already struggling to find skilled workers, which means talent shortage poses a significant challenge. As a smaller company situated on the outskirts of Munich, Germany, we are not immune to the impacts of this shortage. To tackle this challenge as a community, we would like to share a couple of strategies we use to address talent scarcity.

### Investing in the new generation

We recognize the importance of nurturing talent from the ground up, so ERS places a strong emphasis on recruiting students through comprehensive internship programs. Every year, ERS onboards 4-5 longer-term interns from various universities. We have worked with universities abroad in Vancouver, Dubai, and Paris, but are also focusing our efforts on building partnerships with universities here in Germany.

These internships go beyond the traditional coffee-fetching roles, providing hands-on experiences on real-world projects. By immersing students in our daily operations, we offer a unique opportunity for them to gain practical skills and a genuine feel for working at a



As the future of hiring continues to change and the talent pool for the semiconductor industry remains strained, Onto Innovation remains focused on our current talent to ensure they feel supported in their growing career at Onto, leaving us with high employee satisfaction and an environment where newcomers want to join.

company in the semiconductor industry. This approach not only allows us to identify and nurture potential long-term talents but also fosters a culture of innovation and creativity. As these students grow within the company, they become integral parts of our workforce, contributing to our success while simultaneously addressing the talent shortage.

In our commitment to investing in the new generation, we organize and participate in several events annually, extending invitations to school classes or smaller groups of pupils to explore our headquarters and production facilities. To effectively address the challenge of the global talent shortage over the longer term, it is crucial to expose young people to diverse career and job prospects within our industry.

### Local engagement and brand-building

Understanding the importance of a strong local presence, our company actively engages with the community in different ways. We sponsor and collaborate with local organizations, for example, the local soccer and ice hockey teams. This fosters an awareness of our presence in the neighborhood and the exciting opportunities within our company and helps us create a positive brand image and tap into the local talent pool.

Since last year, we have also actively worked with the city council and other community actors on a campaign to promote the location as a business capital. This initiative goes beyond just finding talent, as it contributes to the overall economic development of the area.

Embracing a comprehensive strategy, these are some of the ways we have tackled the global talent shortage. By investing in students and young people, and actively engaging with the local community through collaborations with the city council and various stakeholders, we can quickly adapt to a rapidly growing industry.

## Think Globally, Act Locally

By Paul Ballentine, Mosaic Microsystems



In addressing the global semiconductor talent shortage, Mosaic Microsystems' approach is to think globally and act locally. We aim to become a leading worldwide supplier of glass interposers to the semiconductor industry by building on the considerable ecosystem in Rochester, NY, where a talented labor pool and top-notch colleges and universities exist.

Our approach consists of five parts. The first is to work with local and regional educational institutions to ensure an adequate supply of employees with the right skills, at the right levels, in the right numbers, and at the right time. This includes people with 2-year, bachelor's, and graduate degrees.

Mosaic has close ties with the University of Rochester and the Rochester Institute of Technology and already employs people who have graduated from both schools. RIT is an essential partner due to its Microelectronics Department, which is the first of its kind in the country, and its co-op program, which allows companies to hire college students temporarily and, if they are a good fit, hire them full-time once they graduate. RIT is also one of only six universities in the U.S. that is a member of the U.S.-Japan University Partnership for Workforce Advancement and Research & Development in Semiconductors for the Future (UPWARDS).

At the 2-year level, Mosaic will be working with Monroe Community College, which is the largest community college in Upstate New York and has two existing manufacturing programs that could be relevant: Optics Manufacturing and Precision Machining. Beyond the

Rochester area, four regional universities can provide us with well-trained students: Rensselaer Polytechnic Institute, Clarkson University, Cornell University, and Binghamton University. In addition to recruiting from these universities, we also have collaborations such as SBIR/STTR grants. This helps familiarize students with our technology so they can hit the ground running should they become employees.

The second part is to recruit from the existing labor pool in Rochester which consists of many highly trained and

experienced people who used to work for companies like Kodak and Xerox. Across Upstate New York there are people with experience in semiconductors from companies like IBM and GlobalFoundries.

The third part of the plan is to work with local community organizations such as RochesterWorks to help the economically disadvantaged and unemployed find jobs.

The fourth part of our plan is to provide on-the-job training and continuing education opportunities for existing employees through mentoring and professional development courses.

The fifth part is to reach out to local public schools — particularly the Rochester City School District, which has a high percentage of poor and disadvantaged students — to teach the students about opportunities in semiconductor manufacturing to develop a pipeline of future employees.

Having a high concentration of educational institutions with programs relevant to semiconductor manufacturing, a large workforce skilled in manufacturing, and a large underserved—and untapped—population will enable Mosaic to achieve its goal of having a well-trained and diversified workforce that supports our growth plans.

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## ISS Europe 2023

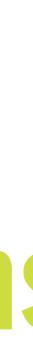
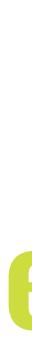
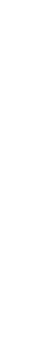


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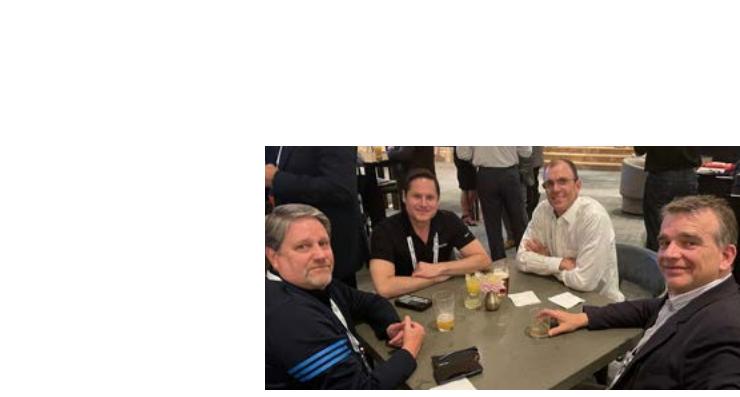


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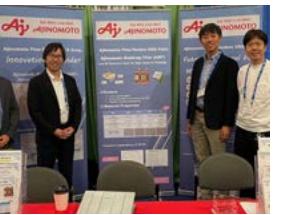
# CHIPCon 2023

# SEMI Women in Semiconductors





# IMAPS Symposium 2023





# SEMICON Europa





# The Role of 200mm Manufacturing in Enabling a \$1 Trillion Semiconductor Industry

Continued from page 11

## Material Matters

Materials play a critical role in the semiconductor industry and can significantly impact its ability to reach a \$1 trillion valuation. As energy efficiency becomes increasingly important in electronic devices and data centers, materials that reduce power consumption are vital. SiC and GaN both help to improve energy efficiency and reduce heat generation. In addition to compound semiconductors, materials like high-k dielectrics are essential for achieving smaller transistor sizes and higher performance.

Whereas 300mm manufacturing is defined by geometry, 200mm and below is defined by materials innovation. Our focus is not on 7nm/5nm line widths but on, for example, obtaining SiC wafers with low defects. Implementing metal-organic chemical vapor deposition (MOCVD) and stacking materials to obtain the best performance are key material challenges that we look at in the non-300mm arena. GaN as the next alternative for power devices has not yet ramped up, but transitioning from silicon and SiC to volume GaN production will

present new challenges. Regardless, power electronics are on a strong growth surge – Yole Group predicts that the market will reach \$33.3 billion in 2028 with a CAGR of 8.1%.

## Strategic Contributors in 200mm Manufacturing and Beyond

Companies like Plasma-Therm that have consistently focused on sub-200mm manufacturing are well positioned against the current technological and geopolitical backdrop. While those in the 300mm space are thinking about 200mm, we have built our business by centering it around 200mm and below. Rather than dabbling in SiC to take advantage of the power trend or as a means of downshifting to 200mm, we have strategically targeted this sector from the beginning. We're making strategic contributions to elevating the visibility of 200mm manufacturing and below as its role in helping drive the semiconductor industry toward that \$1 trillion market continues to gain momentum. 



## 3D InCites Member Stammtisch 2023



## Driving Into the Future

Continued from page 21

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# Five Workflows for Tackling Heterogeneous Integration of Chiplets for 2.5D/3D

**Continued from page 27**

This intensive level of analysis requires detailed thermal chip models. The models need to account for power density and transistor level heating at the die level, and assuming uniform temperature across the die is no longer realistic.

Mechanical stress can also be an issue given the substrate size and different materials used. For example, with a large, multi-reticle silicon interposer sitting on an organic package substrate, the analysis must account for different coefficients of thermal expansion values and must evaluate effects like thermally induced bump stress or substrate warpage.

Design for manufacturing and electrical rule checks also need to be performed at both the chiplet and SiP levels. These include checks for electromigration, electrostatic discharge, latch-up, and electrical over-stress. To expedite this type of SiP analysis, the required chiplet models and performance data should be included in their respective design kits.

## Test Planning and Validation

Perhaps one of the more challenging workflows for HI is manufacturing test, as it requires design for test (DFT) infrastructure, wafer-level test, die test in package, and interface testing between the dies.

The good news is that there are established DFT standards for testing 2.5D and 3D designs, including IEEE standards 1838, 1687, and 1149.1. Additionally, this workflow is supported by recent DFT advancements like memory testing and built-in self-test (MBIST) with 1838 compliant test access ports; scan testing that supports a 3D package pattern retargeting flow; and die-to-die interconnect testing using differential wearing scheme chains composed of wrapper cells. These methods must be designed early to support SiP testing; this requires planning at the package

level for probe pad access and test IO—similar to planning requirements for high-speed IOs.

As well, it is imperative to understand that test considerations cannot wait until the end of the design flow and must also be incorporated into early planning. Packaging engineers must collaborate with test engineers to develop the test IO plan and support static timing analysis and timing simulation requirements.

## Multi-Domain Co-Design Unlocks the Benefits of HI

Successful delivery of heterogeneously integrated systems requires integrated, multi-domain workflows and collaborative design methods throughout the entire design lifecycle.

Heterogeneous design generates a tremendous amount of multi-domain data spanning the entire product lifecycle. This necessitates managing a design database for the system, RTL, silicon, and even mechanical design. HI design also includes a broad spectrum of IP, materials, and design kits. All this data needs to be carefully managed and synchronized to ensure efficiency and design integrity throughout the design process.

There are numerous advantages and benefits of heterogeneous integration. It enables larger, more complex systems than monolithic SoCs and offers improved power, performance, area, and form factors. However, these benefits do not come for free. There are key challenges that must be met, including optimal decomposition and architecture selection, power delivery through the system, as well as thermal management, timing, and test. Companies that want to overcome the challenges and reap the full benefits of HI design should focus their efforts on building, qualifying, and deploying the five workflows presented in this article. 

## Intern Essay Contributors

**Continued from page 5**



**Erwan Amade**, author of *Navigating the World of Semiconductors: My Journey at Megatech*, is a 4th year student intern at Megatech. At the age of 21, he studied Chemical and Process Engineering at Lyon 1 and acquired technical expertise at CEA Leti in Grenoble with Entegris for an internship. He then joined Hybria to specialize in commercial engineering. He's passionate about technology and business, and his academic career reflects this convergence.



**Mindy Lok**, author of *Learning About Strategic Semiconductor Communication: My Internship at Kiterocket* is a student intern at Kiterocket, a global PR and marketing agency with extensive experience across the technology and sustainable living sectors. She is a senior studying public relations with a minor in digital audiences at Arizona State University. She strives to grow and expand her skills as a strategic communicator and digital marketer within business and technology.

# The Year in Test

**Continued from page 39**

At IEEE ITC in October 2023, Cariad (the electronics arm of Volkswagen) pointed out that testing for ADAS L4 and L5 environments generates a lot of data that, at present, is a missed opportunity for analysis/action. The unification of ATE tests would eliminate the overlap and duplication that come from how test was historically done, with batteries of tests from silos of R&D, quality assurance, security, and product/test/design organizations.

## Can We Eliminate Silent Data Corruptions?

All these advances in testing and unification are nice—but why are very subtle, silent data corruptions (SDC) still happening in the field? Is the answer more testing? They are silent and even if the mechanism is discovered, then additional testing adds expense.

At IEEE ITC 2023, there was an excellent panel discussion on SDC about how to catch them in manufacturing, do advanced defect models, improve screening, and the benefits of telemetry. Overall, two main causes were highlighted: Good old-fashioned random points defects and more systemic parametric type failures within complex designs.

The point defects can be time zero test escapes or defects that just require a little bit of 'activation' time to emerge. Can more "intelligent" high voltage tests be invoked? The more sinister examples, although

parametric in nature, involve very small delay effects and/or voltage droops under complex power schemes and situations. It begs the question—can more be done in design/validation to cover proper IC workloads? More specifically, if a part is said to be "pass" or "fail", then the entire condition set needs to be understood ie: at what frequency at what voltage? A multi-layer approach is needed. Should quiescent current testing/fingerprinting be brought back? But after all these efforts—will we merely find the easy mechanisms and the hard ones will continue to elude us?

In summary, the industry drivers, such as automotive, compute, and advanced process/package nodes; combined with the never-ending quest to be smaller, better, faster, and cheaper—continue to result in new test challenges. More "shift left" is needed in test to speed up and improve the quality of development. Standards such as IEEE 1838 and UCIe 1.1 are steps in the right direction. Greater unification is happening across the test process flow, including linking SLT and ATE test more closely, and moving more 'on the fly' analytics to the tester for real-time reaction. Lastly, SDC is on the rise and is very hard to solve in a cost-effective manner. 

1. ["SiC MOSFET Challenges, Demand and Industrialization of Test & Burn-in" – Mark Berry, 3D InCites.](#)
2. ["Update on UCIe" – Mark Berry, 3D InCites, October 2022](#)

## Balancing Precision and Throughput in 3D Structures with Advanced Packaging and Motion Control

**Continued from page 43**

The metrology frame concept also reduces any vibration feedback loop within the system that acts on the tool point, thus minimizing disturbance in the desired placement, process, or inspection steps. As high throughput target placement capabilities in the sub-50 nm realm emerge for heterogeneous chiplet integration strategies, especially when future hybrid bonding processes are considered, a fully integrated motion system including an active isolation platform, multi-axis stage, advanced motion control electronics, and algorithm architecture becomes necessary.

## Conclusion

The semiconductor industry's relentless drive towards 3D structures and emerging advanced packaging techniques to drive "More than Moore's Law" objectives require increasingly more complex, precise, and reliable production processes.

These new developments in the motion control space are permitting manufacturers to meet and exceed these strict precision requirements, whilst still maintaining a more than satisfactory throughput, and cost of ownership. The semiconductor industry will continue to innovate beyond the apparent physical limits of silicon transistor production and manufacture devices at the system level that deliver superior performance coupled with power efficiency, all within a standard package footprint or perhaps extending module package sizes.

Power and heat dissipation from these complex multi-chip systems will continue to challenge the industry as compute demand continues to scale in high-speed AI applications. 

Continued from page 46

Electroplating is an essential AP process, enabling fast, cost-effective formation of electrical features and metallic connections. In addition, electroplating creates a huge opportunity for single-wafer processing systems such as the ClassOne's Solstice® platform. The Solstice LT is an ideal bridge tool from wet bench to single-wafer processing for universities and research institutions. At the same time, the Solstice S4 and S8 models offer students the opportunity to gain experience in programming automation.

Universities are researching technologies such as ultra-high-aspect-ratio through-silicon via (TSV) features on semiconductor wafers and new areas like quantum computing, which uses novel processes and unique materials, such as indium and aluminum. Single-wafer systems can better accommodate these advanced processes and technologies than wet benches.

## Leveraging TDC Expertise

ClassOne has worked with research institutes in Europe, such as Germany's **Fraunhofer ENAS** and **Ferdinand-Braun-Institut**, and **VTT Technical Research Centre of Finland**, as well as **3IT at Université de Sherbrooke** in Canada. The company has also established relationships with several leading U.S. universities, including **Georgia Institute of Technology**, which is at the forefront of addressing the nation's need for semiconductors.

A key aspect of this is the collaborative development efforts pursued in ClassOne's **Technology Development Center (TDC)**, where company engineers process customer wafers, develop and execute process experiments, and devise new products and enhancements to established tools. Customers can take advantage of technical training and demonstrations, while ClassOne expands its depth of knowledge

via projects being pursued by universities, institutions, and corporate customers.

In conclusion, the semiconductor industry stands at a crucial juncture, marked by unprecedented demand for its products and an acute shortage of skilled professionals. The need for semiconductor firms to actively engage in programs that entice college students to join the industry cannot be overstated. The future of technology, from AI and autonomous vehicles to renewable energy solutions and healthcare advancements, depends on a robust and innovative semiconductor sector.

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<b>Semi</b>	semi.org	.....	<b>10</b>	<b>Mosaic Microsystems</b>	mosaicmicro.com	.....	<b>49</b>
<b>Amkor</b>	amkor.com	.....	<b>12</b>	<b>KLA</b>	kla.com	.....	<b>73</b>
<b>Siemens</b>	siemens.com	.....	<b>16</b>	<b>IMAPS</b>	imaps.org	.....	<b>74</b>
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Sitaraman (Sita) Balasubramanian - Aptiv  
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## Post Conference Events - Thursday, March 21

### GOLF

4-Person Scramble  
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### HIKING

12:30 PM - 5:00 PM

For the third consecutive year, 3D InCites will be holding their Hike for the DEI fundraiser. 100% of the proceeds benefit the 3D InCites DEI Fund; this fund is used to establish a DEI Scholarship to help young women and under-represented minorities gain access to STEM education programs at the technical school, community college and university levels.

This guided, 2-hour afternoon hike takes place in the McDowell Mountains in Fountain Hills Arizona, as part of the 2024 IMAPS Device Packaging Conference.

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